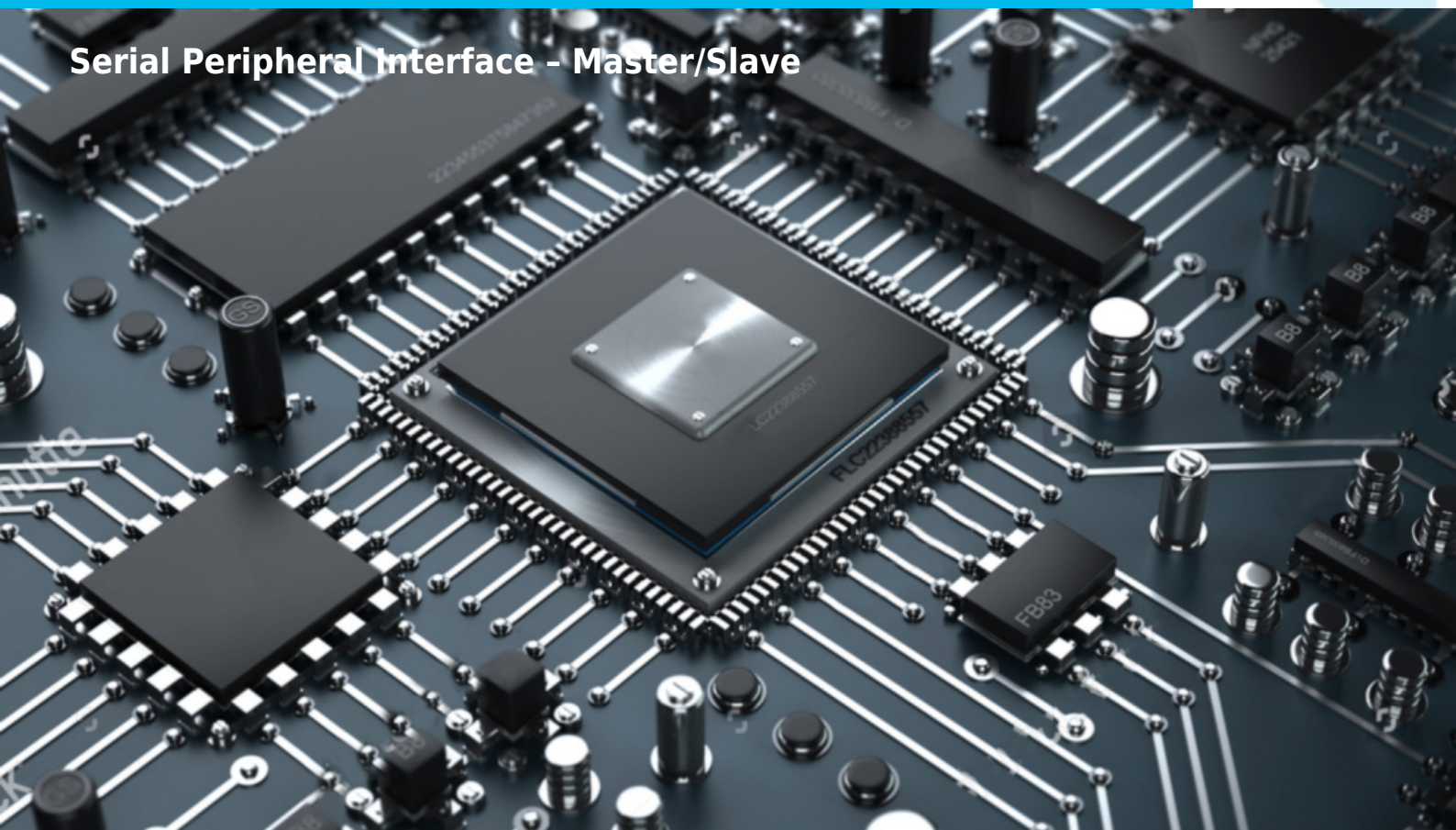
DIGITAL CORE DESIGN

DSPI

Serial Peripheral Interface – Master/Slave



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DSPI SPI IP Core – High-Performance, Configurable SPI Master/Slave for SoC and FPGA Designs

The **DSPI IP Core** from DCD-SEMI is a high-performance, fully configurable SPI master/slave controller, bridging seamlessly to **APB, AHB, and AXI bus interfaces**. Designed for flexible system integration, it allows engineers to configure **serial clock (SCK) polarity and phase**, enabling robust communication between microcontrollers and serial peripheral devices.

Optimized for **multi-master systems**, the DSPI controller supports interprocessor communications and simultaneous data transmission and reception on two independent serial data lines. Its **technology-independent design** allows implementation across a variety of process technologies, making it ideal for FPGA and ASIC integrations.

The DSPI system is compatible with a wide range of peripheral devices from multiple manufacturers. It supports master or slave configurations with data rates of up to **CLK/4**, and its clock control logic accommodates multiple SPI protocols, ensuring compatibility with most synchronous serial peripherals.

Key features include:

- **Automatic Slave Select Control (SSCR)** for deterministic device addressing
- **Eight selectable SPI clock bit rates** for flexible system timing
- **Error detection logic** supporting interprocessor communications
- **Write-collision detection** to prevent data corruption during transfers
- **Multi-master fault protection** automatically disables output drivers if bus contention occurs
- **Fully customizable** IP delivered tailored to your system configuration, reducing unused features and wasted silicon

The DSPI IP Core includes a **complete automated test bench**, enabling rapid validation at every stage of the SoC design flow. Its combination of **high configurability, reliability, and performance** makes it the perfect SPI solution for embedded, SoC, and FPGA-based designs.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

DCD-SEMI SPI IP Cores

	DSPI	DQSPI	DOSPI	DFSPI	DOSPIS	DESPI	DESPIS
SPI mode	SINGLE	SINGLE, DUAL, QUAD	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD	SINGLE, DUAL, QUAD
Operation mode	Master only	Master only	Master only	Master only	Slave only	Master only	Slave only
Data rate	Low	Middle	High	High	High	Middle	Middle
Cost / complexity	Low	Middle	Middle	High	Middle	High	High
XIP support	Optional	Optional	Optional	Yes	No	No	No
DDR support	Yes	Yes	Yes	Yes	No	No	No
Standard supported	xSPI partially	xSPI partially	xSPI partially	xSPI, HyperBus, XCELLA	xSPI partially	Intel eSPI 1.6	Intel eSPI 1.6
Best option for	Memory controller, SPI peripheral controller i.e. sensors	Memory controller, SPI peripheral controller i.e. sensors	Memory controller, SPI peripheral controller i.e. sensors	Memory controller (Flash, DRAM, PSRAM, HyperRAM and other), program code execution	Serial bus to parallel bus bridge, RAM connection to SPI interface	PC mother-boards	PC mother-boards

KEY FEATURES

- **SPI Master**
  - Master and Multi-master operations
  - 8 SPI slave select lines
  - System error detection
  - Mode fault error
  - Write collision error
  - Interrupt generation
  - Supports speeds up 1/4 of system clock
  - Bit rates generated 1/4 – 1/512 of system clock.
  - Four transfer formats supported
  - Simple interface allows easy connection to microcontrollers
- **SPI Slave**
  - Slave operation
  - System error detection
  - Interrupt generation
  - Supports speeds up 1/4 of system clock

Copyright © 1999 - 2026 DCD - DCD-SEMI Sp. z o.o. All Rights Reserved.
All trademarks mentioned in this document are the property of their respective owners.

- Simple interface allows easy connection to microcontrollers
- Four transfer formats supported
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready

UNITS SUMMARY

SPI Clock logic – Controls phase and polarity of the SCK clock line. In the same time it detects correct sample and shift edge for the Shift register. SPI Clock Logic allows user to select any of four combinations of serial clock (SCK) phase and polarity using two pins CPHA and CPOL. The clock polarity is specified by the CPOL, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase CPHA selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPIS allows direct interface to almost any existing synchronous serial peripheral. **Shift register** – The central element in the SPI system. When SPI transfer occurs, an 8-bit character is shifted out on data pin while a different 8-bit character is simultaneously moved in a second data pin. Another way to view this transfer is when an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is moved 8-bit positions. Moreover, the characters in the master and slave are effectively exchanged. **Data Register** – Holds data read from passive device, to be sent serially to the SPI Master. **Address Register** – Holds address presented on Address bus. Its contents are incremented every single data portion sent/ received serially through the SPI bus. **SPI Controller** – Detects the beginning and end of SPI transfer. Manages data exchange between DSPIS and a passive device controlled by DSPIS and increments Address Register (SPAD) after any successful transfer.

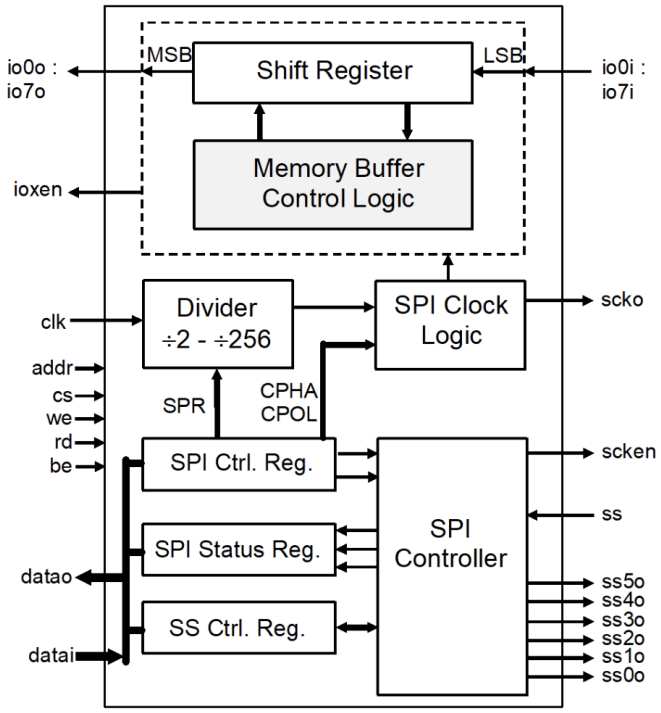
TRANSFER FORMATS

The software can select any of four combinations of serial clock (SCK) phase and polarity, using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI, allows direct interface to almost any existing synchronous serial peripheral.

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Digital multimeters

BLOCK DIAGRAM



PERFORMANCE

The following table gives a survey about the Core area and performance in **LATTICE FPGA** devices after Place & Route (all key features included):

Device	Speed grade	LUTs/PFUs	F_{max}
XP	-5	94 / 55	219 MHz
ECP	-5	94 / 55	226 MHz
EC	-5	94 / 55	222 MHz
XP2	-7	69 / 49	306 MHz
ECP2	-7	90 / 55	324 MHz
ECP2M	-7	69 / 49	345 MHz
SC	-7	84 / 55	489 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

Copyright © 1999 - 2026 DCD - DCD-SEMI Sp. z o.o. All Rights Reserved.
All trademarks mentioned in this document are the property of their respective owners.

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

DCD-SEMI Sp. z o.o. Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/

Copyright © 1999 - 2026 DCD - DCD-SEMI Sp. z o.o. All Rights Reserved.
All trademarks mentioned in this document are the property of their respective owners.