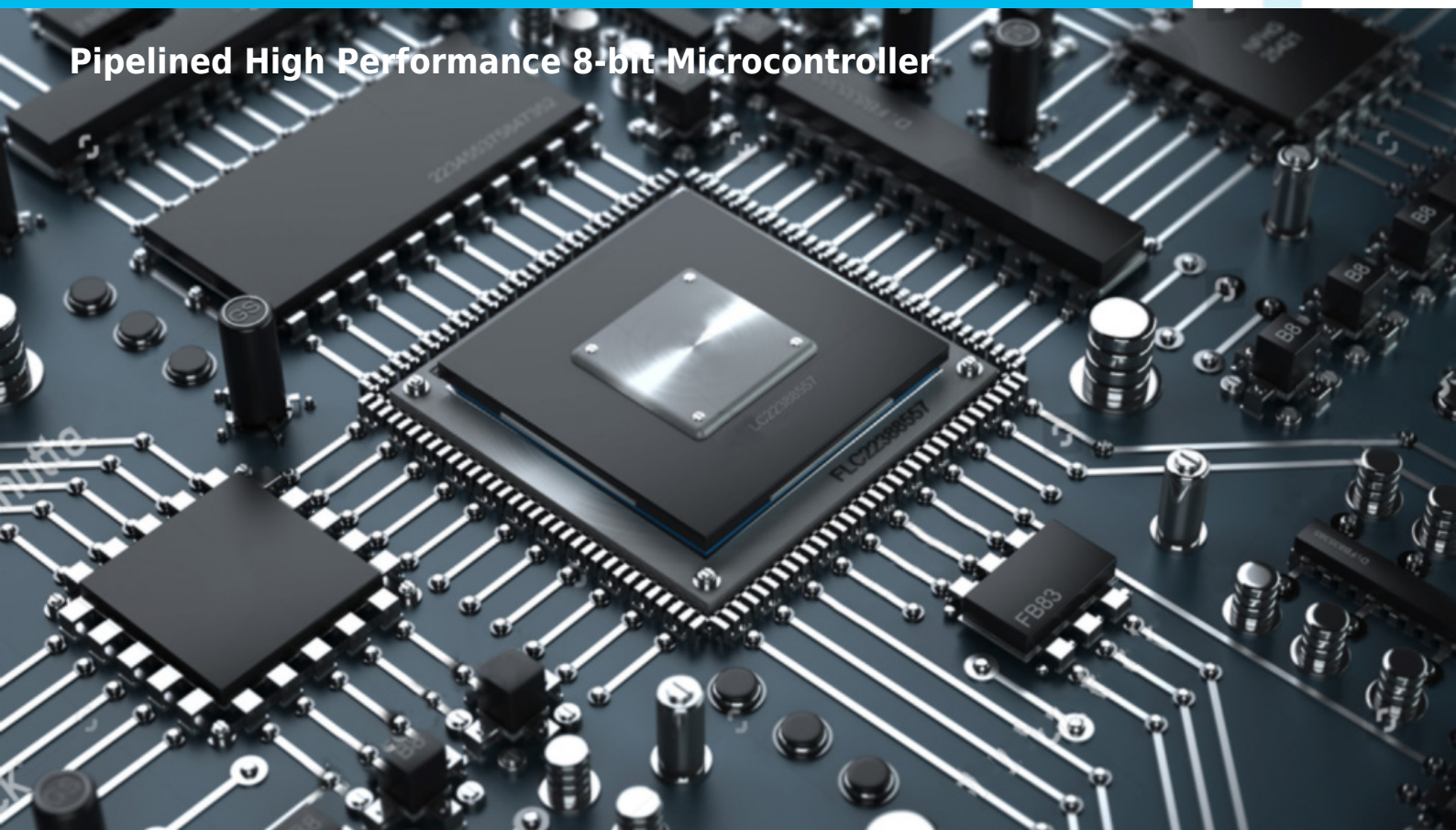
DIGITAL CORE DESIGN

DP80390CPU

Pipelined High Performance 8-bit Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DP80390CPU is an **ultra-high performance**, **speed-optimized** soft core of a single-chip, 8-bit embedded controller, intended to operate with fast (typically on-chip) and slow (off-chip) memories. The core was designed with a special concern about the performance to power-consumption ratio. It supports up to 8 MB of linear code space and 16 MB of linear data space. This ratio is extended by an **advanced power management (PMU) unit**. The DP80390CPU softcore is 100% binary-compatible with the industry standard 80390 & 8051 8-bit microcontroller. There are two configurations of DP80390CPU:

- Harvard, where internal data and program buses are separated, and
- von Neumann, with common program and external data bus

The DP80390CPU has a Pipelined RISC architecture and executes 85-200 million instructions per second. **Dhrystone 2.1 benchmark program runs from 11.46 to 15.55 times faster than the original 80C51 at the same frequency.** The same C compiler was used for benchmarking of the 80C51 core with the same settings. This performance can be also exploited to great advantage in low-power applications, where the core can be clocked over ten times slower than the original implementation, without performance depletion. The DP80390CPU is delivered with a **fully automated test bench** and a **complete set of tests**, allowing easy package validation at each stage of the SoC design flow. Each of DCD's 80390 Cores has built-in support for the proprietary Hardware Debug System, called **DoCD™**. It is a **real-time hardware debugger**, which provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides **non-intrusive debugging** of a running application. It can halt, run, step into or skip an instruction, and read/write any contents of the microcontroller, including all registers, internal and external program memories, and all SFRs, including user-defined peripherals.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.
- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

CPU FEATURES

- software in 100% compatible with 80390 & 8051 industry standards
  - LARGE mode – 8051 instruction set
  - FLAT mode – 80390 instruction set
- Pipelined RISC architecture enables to run 15.55 times faster, than the original 80C51 at the same frequency
- Up to 14.632 VAX MIPS at 100 MHz
- 24 times faster multiplication
- 12 times faster division
- Up to 256 bytes of internal (on-chip) Data Memory
- **Up to 8 MB of linear Program Memory**
  - 64 kB of internal (on-chip) Program Memory
  - 8 MB external (off-chip) Program Memory
- Up to 16 MB of external (off-chip) Data Memory
- User programmable Program Memory Wait States
- User programmable External Data Memory Wait States
- De-multiplexed Address/Data bus, to allow easy memory connection
- Interface for additional Special Function Registers
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- 2 GHz virtual clock frequency in a 0.25u technological process
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

PROGRAM MEMORY:

The DP80390 soft core is dedicated to operate with Internal and External Program Memory. It maximal linear size is equal to 8 MB. Internal Program Memory can be implemented as:

– ROM located in address range between 0x0000 ¸ (ROM_{size}-1)
– RAM located in address range between (64kB-RAM_{size}) ¸ 0xFFFF

External Program Memory can be implemented as ROM or RAM, located in address range between ROM_{size} ¸ 8 MB excluding area occupied by RAM_{size}.

INTERNAL DATA MEMORY:

The DP80390CPU can address Internal Data Memory of up to 256 bytes The Internal Data Memory can be implemented as Single-Port synchronous RAM.

EXTERNAL DATA MEMORY:

The DP80390CPU soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

USER SPECIAL FUNCTION REGISTERS:

Up to 104 External (user) Special Function Registers (ESFRs) may be added to the DP80390CPU design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

WAIT STATES SUPPORT:

The DP80390CPU soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory Wait signal to hold up CPU activity.

PERIPHERALS

- **DoCD™ debug unit**
  - Processor execution control
    - Run
    - Halt
    - Step into instruction
    - Skip instruction
  - Read-write all processor contents
    - Program Counter (PC)
    - Program Memory
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Code execution breakpoints
    - up to eight real-time PC breakpoints
    - unlimited number of real-time OPCODE breakpoints
  - Hardware execution watchpoint
    - one at Internal (direct) Data Memory
    - one at Special Function Registers (SFRs)
    - one at External Data Memory
  - Hardware watchpoints activated at certain:
    - address by any write into memory
    - address by any read from memory
    - address by write into memory required data
    - address by read from memory required data
  - Unlimited number of software watch-points
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Unlimited number of software breakpoints
    - Program Memory(PC)
  - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
  - TTAG or JTAG Communication interface
- **Power Management Unit**
  - Power management mode
  - Switchback feature
  - Stop mode
- **Interrupt Controller**
  - 2 priority levels
  - 2 external interrupt sources

UNITS SUMMARY

ALU – Arithmetic Logic Unit – performs arithmetic and logic operations during execution of an instruction. Contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.
Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.
Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and manages execution of all microcontroller tasks.
Program Memory Interface – Contains Program Counter (PC) and related logic. Performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C and DoCD™ module.
External Memory Interface – Contains memory access related registers, such as Data Page High (DPH), Data Page Low (DPL) and Data Page Pointer (DPP) registers. Performs external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by the user. This feature is called Program Memory Wait States and it allows core to work with different speed program memories.
Synchronous eXternal Data Memory (SXDM) Interface – Contains XDATA memory access related logic, allowing fast access to synchronous memory devices. It performs the external Data Memory addressing and data transfers. This memory can be used to store large variables, frequently accessed by the CPU, improving overall performance of application.
Internal Data Memory Interface – Controls the access into internal memory of size up to 256 bytes. Contains 8-bit Stack Pointer (SP) register and related logic.
User SFRs Interface – Special Function Registers interface controls access to special registers. Contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.
Interrupt Controller – Responsible for the interrupt manage system of the external and internal interrupt sources. Contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers.
Power Management Unit – Contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in a full speed mode, if enabled. It is highly desirable, when the

microcontroller is planned to be used in portable and power critical applications.

DoCD™ Debug Unit – it's a **real-time hardware debugger**, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DEBUGACS, indicate the state of the debugger and CPU. The CODERUN is active when the CPU is executing an instruction. The DEBUGACS pin is active when any access is performed by **DoCD™** debugger. The **DoCD™** system includes **TTAG** or **JTAG interface** and complete set of tools, to communicate and work with the core in real time debugging. It is built as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to a power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off.

CONFIGURATION

The following parameters of the DP80390CPU core can be easily adjusted to requirements of dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Internal Program Memory type: *synchronous / asynchronous*
- Internal Program ROM Memory size: *0 – 64kB*
- Internal Program RAM Memory size: *0 – 64kB*
- Internal Program Memory fixed size: *true / false*
- Interrupts: *subroutines location*
- Power Management Mode: *used / unused*
- Stop mode: *used / unused*
- **DoCD™** debug unit: *used / unused*

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

PERFORMANCE

The following table gives survey about the Core area and performance in **ASIC** Devices (CPU features and peripherals included):

Technology / optimization	Speed grade	Area [gates]	F_{max}
0.25u area	typical	6 550	100 MHz
0.25u speed	typical	8 220	250 MHz
0.18u area	typical	6 200	100 MHz
0.18u speed	typical	7 470	300 MHz

Core performance in ASIC devices – results given for working system with IDATA, CODE and XDATA memories. The DoCD debugger increases the core size by about 2 200 gates.

For the user, the key factor is an application speed improvement. The most commonly used arithmetic functions and their improvement are shown in the following table. The improvement was computed as {80C51 clock periods} divided by {DP80390CPU clock periods} required to execute an identical function. More details are available in the core documentation.

Function	Improvement
8-bit addition (*immediate data*)	**9,00**
8-bit addition (*direct addressing*)	**9,00**
8-bit addition (*indirect addressing*)	**9,00**
8-bit addition (*register addressing*)	**12,00**
8-bit subtraction (*immediate data*)	**9,00**
8-bit subtraction (*direct addressing*)	**9,00**
8-bit subtraction (*indirect addressing*)	**9,00**
8-bit subtraction (*register addressing*)	**12,00**
8-bit multiplication	**16,00**
8-bit division	**9,60**
16-bit addition	**12,00**
16-bit subtraction	**12,00**
16-bit multiplication	**13,60**
32-bit addition	**12,00**
32-bit subtraction	**12,00**
32-bit multiplication	**12,60**
Average speed improvement:	**11,12**

Dhrystone Benchmark Version 2.1 was used to measure the core performance. The following table shows the DP80390 performance in VAX MIPS per 1 MHz rating.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
DP80390	0,10787	11,46
DP80390+DPTRs	0,13722	14,58
DP80390+DPTRs+SXDM	0,14457	15,36
DP80390+DPTRs+SXDM+MDU32	0,14632	15,55

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist

- Netlist for selected FPGA family
- Sample FPGA project
- Technical documentation
  - HDL core specification
  - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

Digital Core Design Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/