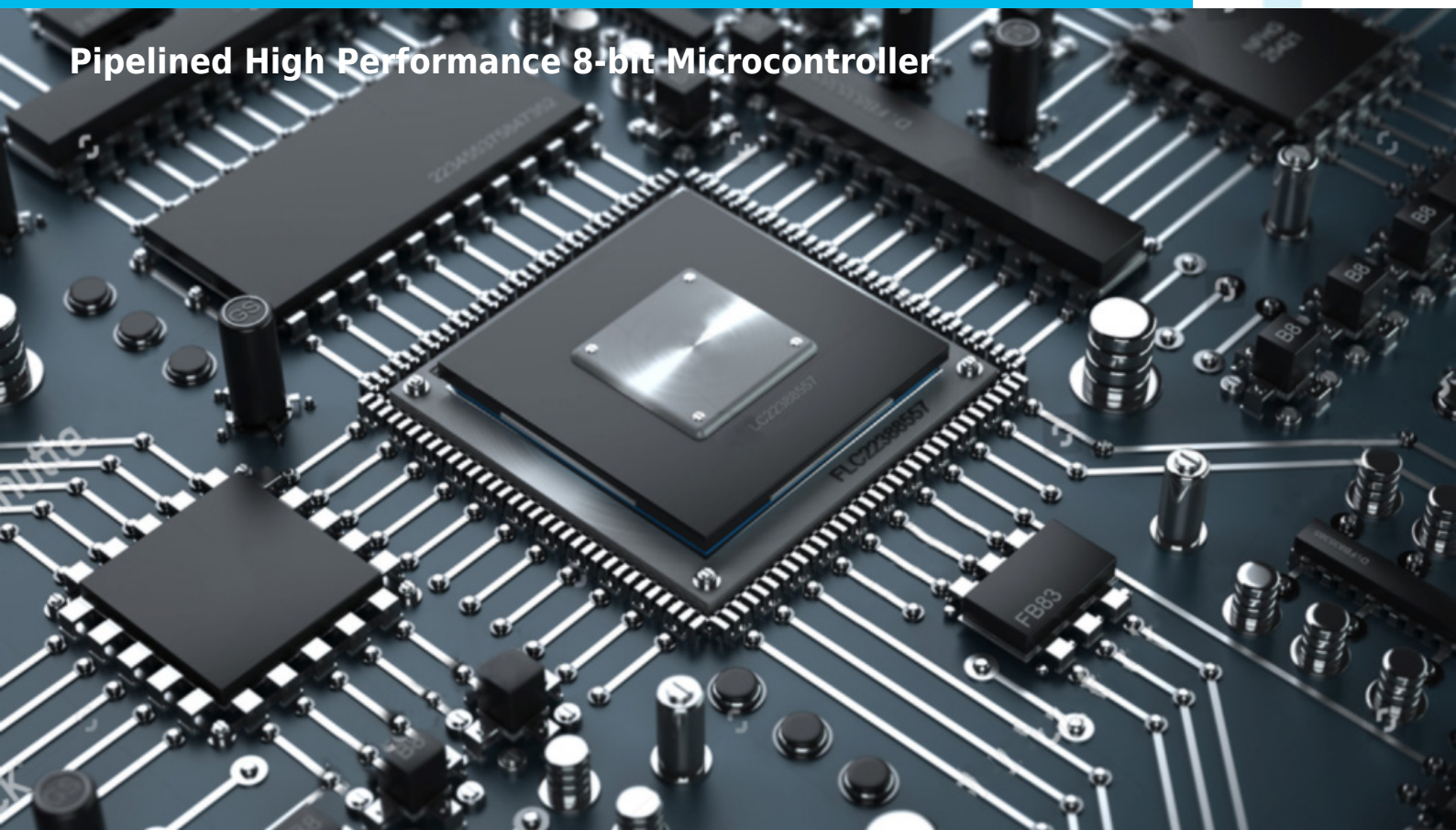
DIGITAL CORE DESIGN

DP80390CPU

Pipelined High Performance 8-bit Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DP80390CPU – HIGH-PERFORMANCE 8-BIT EMBEDDED CONTROLLER IP CORE

The **DP80390CPU** is an **ultra-high-performance, speed-optimized 8-bit soft microcontroller IP core**, designed for **single-chip embedded SoC implementations** operating with both **fast on-chip memories** and **slower off-chip memory devices**. The core is optimized for an exceptional **performance-to-power-consumption ratio**, making it ideal for **low-power, cost-sensitive, and performance-critical embedded applications**.

The architecture supports up to **8 MB of linear program (code) space** and **16 MB of linear data space**, significantly extending the addressing capabilities beyond traditional 8051-based designs. Power efficiency is further enhanced by an **advanced Power Management Unit (PMU)**, enabling aggressive clock scaling without loss of performance.

100% Binary Compatibility with 80390 / 8051

DP80390CPU is **fully binary-compatible** with the industry-standard **80390 and 8051 8-bit microcontroller architectures**, allowing seamless reuse of existing firmware, toolchains, and legacy software investments.

Flexible System Architectures

The core is available in two architectural configurations to match different SoC integration strategies:

- **Harvard Architecture** – separate internal program and data buses for maximum throughput
- **von Neumann Architecture** – shared program and external data bus for simplified system design

High-Performance Pipelined RISC Architecture

DP80390CPU features a **pipelined RISC microarchitecture**, delivering performance levels far exceeding classic 8-bit MCUs:

- **85 to 200 MIPS**, depending on configuration and target frequency
- **Dhrystone 2.1 performance**: **11.46× to 15.55× faster** than the original **80C51** running at the same clock frequency
- Benchmarked using the **same C compiler and identical compilation settings**, ensuring fair and reproducible results

This performance headroom can be directly leveraged in **ultra-low-power designs**, where the core may be clocked **over 10× slower** than legacy implementations while maintaining equivalent application performance.

SoC-Ready Verification and Debug Support

The DP80390CPU is delivered with a **fully automated testbench and a comprehensive regression test suite**, enabling **fast IP qualification and validation** across all stages of the SoC design flow.

Each DP80390CPU core includes built-in support for **DoCD™ (Digital Core Design on-Chip Debugger)** — a proprietary **real-time hardware debug system** providing **non-intrusive debugging** of a live SoC. Unlike traditional on-chip debuggers, DoCD™ allows full system visibility without disturbing application execution.

DoCD™ capabilities include:

- Run, halt, single-step, step-over, and instruction skipping
- Read/write access to **all registers**, **SFRs**, and **user-defined peripherals**
- Full visibility into **internal and external program and data memories**
- True **non-intrusive debugging** of real-time embedded systems

Key Benefits for Design Engineers

- Drop-in **80390 / 8051 software compatibility**
- Up to **200 MIPS** performance in an 8-bit MCU class

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- **Advanced PMU** for low-power SoC designs
- Harvard or von Neumann architecture options
- Proven **Dhrystone benchmark leadership**
- **Non-intrusive, system-wide hardware debugging**
- SoC-ready delivery with automated verification

DP80390CPU VS. CLASSIC 8051 MICROCONTROLLER

Feature / Parameter	DP80390CPU (DCD-SEMI)	Classic 8051 (e.g. 80C51)
Architecture	Pipelined RISC	CISC
Binary Compatibility	100% 80390 / 8051 compatible	Native
Execution Performance	**85–200 MIPS**	~12 MIPS @ 12 MHz
Dhrystone 2.1	**11.46×–15.55× faster**	Baseline (1×)
Instructions per Cycle	Multiple (pipelined)	1 instruction per 12 clocks
Clock Frequency for Same Performance	**Up to 10× lower**	Higher clock required
Power Efficiency	**Very high (advanced PMU)**	Limited
Power Management	**Integrated PMU**	Minimal / external
Program Memory Space	**Up to 8 MB linear**	64 KB
Data Memory Space	**Up to 16 MB linear**	64 KB
Memory Architecture	Harvard or von Neumann	Harvard
On-Chip Debugging	**DoCD™ non-intrusive real-time debug**	Basic / intrusive
Debug Access	Full SoC, registers, SFRs, memories	Limited
SoC Integration	**Soft IP core (RTL)**	Fixed silicon MCU
Verification	**Automated testbench + test suite**	Device-dependent
Firmware Reuse	**Full legacy reuse**	Native
Target Applications	Industrial, Automotive, IoT SoCs	Legacy embedded designs

Industrial Systems

Designed for **industrial control, automation, and field devices**, DP80390CPU delivers **deterministic real-time performance** with long product lifecycle support. High execution efficiency allows **lower clock frequencies**, reducing power dissipation and EMI, while full 8051 software compatibility protects legacy codebases commonly used in industrial environments.

Ideal for:

- PLC subsystems
- Motor control
- Industrial gateways
- Fieldbus and sensor aggregation SoCs

Automotive Electronics

DP80390CPU is well-suited for **automotive body, comfort, and monitoring systems**, where **predictable behavior, low power, and proven architectures** are essential. The core enables reuse of certified 8051-based software while providing **significantly higher performance headroom** for next-generation automotive SoCs.

Ideal for:

- Body control modules (BCM)
- Lighting and climate controllers
- Automotive sensor hubs
- Mixed-signal automotive ASICs

IoT and Edge Devices

For **IoT nodes and edge devices**, DP80390CPU combines **ultra-low-power operation** with enough performance to handle **communication stacks, security functions, and sensor processing**. Clock-scaling enabled by its high MIPS efficiency makes it especially effective in **battery-powered and energy-harvesting designs**.

Ideal for:

- IoT gateways
- Smart sensors
- Wearables and metering
- Edge AI companion controllers

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ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

CPU FEATURES

- software in 100% compatible with 80390 & 8051 industry standards
  - LARGE mode – 8051 instruction set
  - FLAT mode – 80390 instruction set
- Pipelined RISC architecture enables to run 15.55 times faster, than the original 80C51 at the same frequency
- Up to 14.632 VAX MIPS at 100 MHz
- 24 times faster multiplication
- 12 times faster division
- Up to 256 bytes of internal (on-chip) Data Memory
- **Up to 8 MB of linear Program Memory**
  - 64 kB of internal (on-chip) Program Memory
  - 8 MB external (off-chip) Program Memory
- Up to 16 MB of external (off-chip) Data Memory
- User programmable Program Memory Wait States
- User programmable External Data Memory Wait States
- De-multiplexed Address/Data bus, to allow easy memory connection
- Interface for additional Special Function Registers
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- 2 GHz virtual clock frequency in a 0.25u technological process
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

PROGRAM MEMORY:

The DP80390 soft core is dedicated to operate with Internal and External Program Memory. It maximal linear size is equal to 8 MB. Internal Program Memory can be implemented as:

- ROM located in address range between 0x0000 ¸ (ROM_{size}-1)
- RAM located in address range between (64kB-RAM_{size}) ¸ 0xFFFF

External Program Memory can be implemented as ROM or RAM, located in address range between ROM_{size} ¸ 8 MB excluding area occupied by RAM_{size}.

INTERNAL DATA MEMORY:

The DP80390CPU can address Internal Data Memory of up to 256 bytes The Internal Data Memory can be implemented as Single-Port synchronous RAM.

EXTERNAL DATA MEMORY:

The DP80390CPU soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

USER SPECIAL FUNCTION REGISTERS:

Up to 104 External (user) Special Function Registers (ESFRs) may be added to the DP80390CPU design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

WAIT STATES SUPPORT:

The DP80390CPU soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory Wait signal to hold up CPU activity.

PERIPHERALS

- **DoCD™ debug unit**
  - Processor execution control
    - Run
    - Halt
    - Step into instruction
    - Skip instruction
  - Read-write all processor contents
    - Program Counter (PC)
    - Program Memory
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Code execution breakpoints
    - up to eight real-time PC breakpoints
    - unlimited number of real-time OPCODE breakpoints
  - Hardware execution watchpoint
    - one at Internal (direct) Data Memory
    - one at Special Function Registers (SFRs)
    - one at External Data Memory
  - Hardware watchpoints activated at certain:
    - address by any write into memory
    - address by any read from memory
    - address by write into memory required data
    - address by read from memory required data
  - Unlimited number of software watch-points
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Unlimited number of software breakpoints
    - Program Memory(PC)
  - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
  - TTAG or JTAG Communication interface
- **Power Management Unit**
  - Power management mode
  - Switchback feature
  - Stop mode
- **Interrupt Controller**
  - 2 priority levels

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- 2 external interrupt sources

UNITS SUMMARY

ALU – Arithmetic Logic Unit – performs arithmetic and logic operations during execution of an instruction. Contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.
Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.
Control Unit – Performs the core synchronization and data flow control. This module is directly connected to Opcode Decoder and manages execution of all microcontroller tasks.
Program Memory Interface – Contains Program Counter (PC) and related logic. Performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C and DoCD™ module.
External Memory Interface – Contains memory access related registers, such as Data Page High (DPH), Data Page Low (DPL) and Data Page Pointer (DPP) registers. Performs external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by the user. This feature is called Program Memory Wait States and it allows core to work with different speed program memories.
Synchronous eXternal Data Memory (SXDM) Interface – Contains XDATA memory access related logic, allowing fast access to synchronous memory devices. It performs the external Data Memory addressing and data transfers. This memory can be used to store large variables, frequently accessed by the CPU, improving overall performance of application.
Internal Data Memory Interface – Controls the access into internal memory of size up to 256 bytes. Contains 8-bit Stack Pointer (SP) register and related logic.
User SFRs Interface – Special Function Registers interface controls access to special registers. Contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.
Interrupt Controller – Responsible for the interrupt manage system of the external and internal interrupt sources. Contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers.
Power Management Unit – Contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in a full speed mode, if enabled. It is highly desirable, when the microcontroller is planned to be used in portable and power critical applications.
DoCD™ Debug Unit – it's a **real-time hardware debugger**, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DEBUGACS, indicate the state of the debugger and CPU. The CODERUN is active when the CPU is executing an instruction. The DEBUGACS pin is active when any access is performed by **DoCD™** debugger. The **DoCD™** system includes **TTAG** or **JTAG interface** and complete set of tools, to communicate and work with the core in real time debugging. It is built as a scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to a power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off.

CONFIGURATION

The following parameters of the DP80390CPU core can be easily adjusted to requirements of dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Internal Program Memory type: *synchronous / asynchronous*
- Internal Program ROM Memory size: *0 – 64kB*
- Internal Program RAM Memory size: *0 – 64kB*
- Internal Program Memory fixed size: *true / false*
- Interrupts: *subroutines location*
- Power Management Mode: *used / unused*
- Stop mode: *used / unused*
- **DoCD™** debug unit: *used / unused*

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

PERFORMANCE

The following table gives survey about the Core area and performance in **LATTICE** Programmable Logic Devices after Place & Route (CPU features and peripherals included):

Device	Speed grade	Area	F_{max}
XP	-5	2080 LUT4s	76 MHz
EC	-5	2080 LUT4s	82 MHz
ECP	-5	2080 LUT4s	88 MHz
XP	-7	2020 LUT4s	101 MHz
ECP2	-7	2020 LUT4s	120 MHz
ECP2M	-7	2020 LUT4s	123 MHz
SC	-7	2090 LUT4s	149 MHz

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Core performance in LATTICE® devices – results given for the working system with IDATA, CODE and XDATA memories.

For the user, the key factor is the application speed improvement. The most commonly used arithmetic functions and their improvement are shown in the following table. The improvement was computed as {80C51 clock periods} divided by {DP80390CPU clock periods} required to execute an identical function. More details are available in the core documentation.

Function	Improvement
8-bit addition (*immediate data*)	**9,00**
8-bit addition (*direct addressing*)	**9,00**
8-bit addition (*indirect addressing*)	**9,00**
8-bit addition (*register addressing*)	**12,00**
8-bit subtraction (*immediate data*)	**9,00**
8-bit subtraction (*direct addressing*)	**9,00**
8-bit subtraction (*indirect addressing*)	**9,00**
8-bit subtraction (*register addressing*)	**12,00**
8-bit multiplication	**16,00**
8-bit division	**9,60**
16-bit addition	**12,00**
16-bit subtraction	**12,00**
16-bit multiplication	**13,60**
32-bit addition	**12,00**
32-bit subtraction	**12,00**
32-bit multiplication	**12,60**
Average speed improvement:	**11,12**

Dhrystone Benchmark Version 2.1 was used to measure the core performance. The following table shows the DP80390 performance in VAX MIPS per 1 MHz rating.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
DP80390	0,10787	11,46
DP80390+DPTRs	0,13722	14,58
DP80390+DPTRs+SXDM	0,14457	15,36
DP80390+DPTRs+SXDM+MDU32	0,14632	15,55

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Remote Access license option* – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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