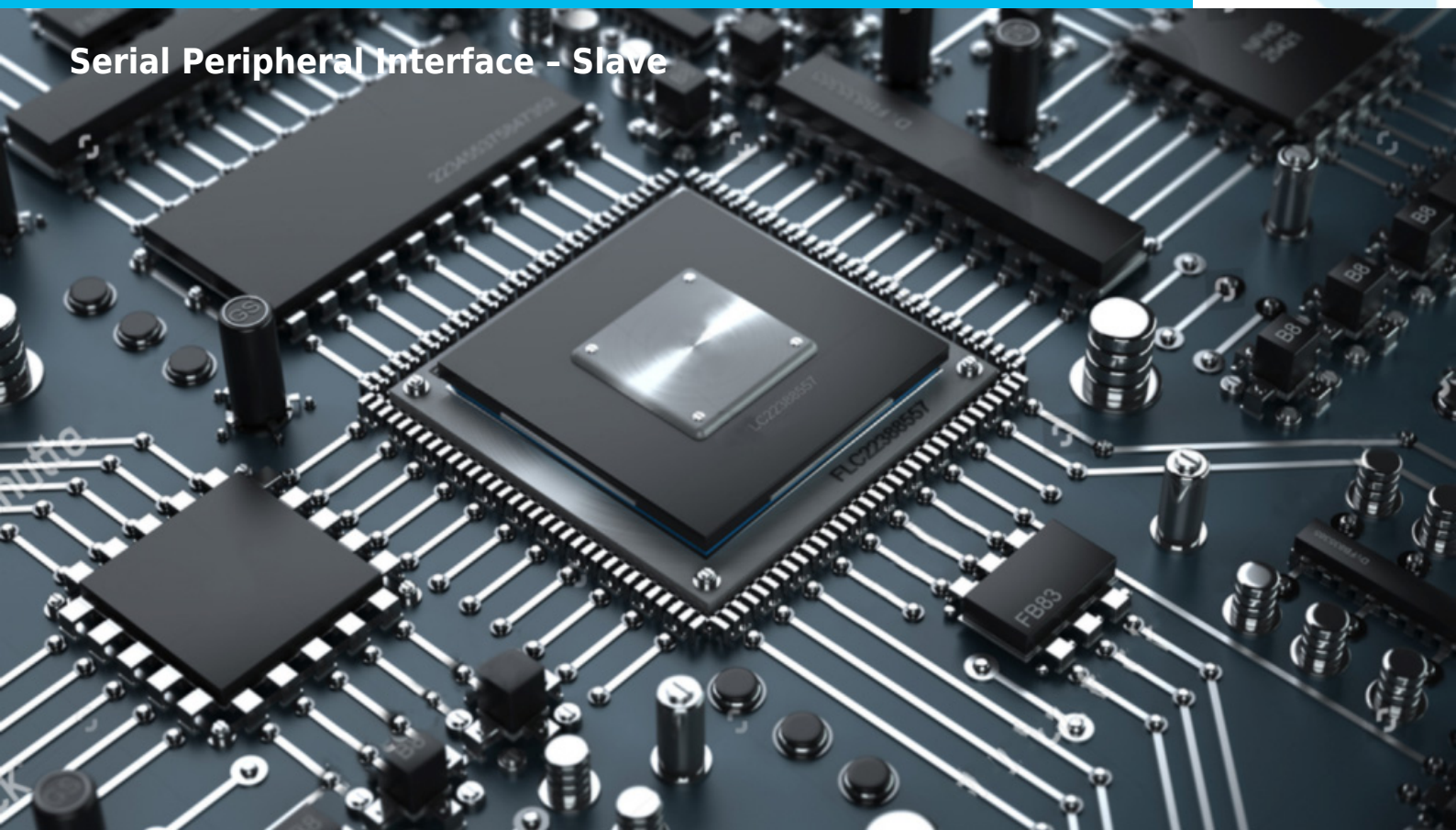
DIGITAL CORE DESIGN

DSPIS

Serial Peripheral Interface – Slave



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DSPIS is a fully configurable **SPI slave device,** designed to **operate with passive devices**, like memories, LCD drivers etc. It allows you to **configure polarity and phase of serial clock signal SCK**. A serial clock line (SCK) synchronizes information shifting and sampling on two independent serial data lines. Moreover, **data is simultaneously transmitted and received**. The DSPIS system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. The clock control logic (**CLK/4**) allows selecting clock polarity and a choosing two fundamentally different clocking protocols, to accommodate most available synchronous serial peripheral devices. The **DSPIS allows the SPI Master to communicate with passive devices**. When transmission starts (SS Line goes low), the first portion of data is copied to the address register and then, to the ADDRESS bus output. After transmission of the address, the DSPIS generates the read signal (RD) and copies DATAI bus contents to the transmitter shift register, and prepares data to be exchanged with the SPI Master. During the next portion of data transmission, the DSPIS simultaneously transfers the data out and in. When the first portion of data is received, the DSPIS asserts DATAO bus generates the write signal (WE), then increments ADDRESS bus performs a read operation and prepare another data portion to be exchanged with SPI master. The transmission is ended when the SS line goes high. The DSPIS is a technology independent design, so can be implemented in variety of process technologies. It's also fully customizable – the configuration is tailored to your requirements. There is no need to pay extra for unused features and wasted silicon. The DSPIs comes with **fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of SoC design flow.

KEY FEATURES

- Full duplex synchronous serial data transfer
- Slave operation
- Automatic read and write operations
- Automatic address incrementation after any data portion transfer
- Configurable address and data length
- Configurable SCK phase and polarity
- Supports speeds up 1/4 of system clock
- Simple interface allows easy connection to passive devices and SPI Master
- Four transfer formats supported
- Simple interface allows easy connection to microcontrollers
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready

UNITS SUMMARY

SPI Clock logic – Controls phase and polarity of the SCK clock line. In the same time it detects correct sample and shift edge for the Shift register. SPI Clock Logic allows user to select any of four combinations of serial clock (SCK) phase and polarity using two pins CPHA and CPOL. The clock polarity is specified by the CPOL, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase CPHA selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPIS allows direct interface to almost any existing synchronous serial peripheral. **Shift register** – The central element in the SPI system. When SPI transfer occurs, an 8-bit character is shifted out on data pin while a different 8-bit character is simultaneously moved in a second data pin. Another way to view this transfer is when an 8-bit shift register in the master and another 8-bit shift register in the slave are connected as a circular 16-bit shift register. When a transfer occurs, this distributed shift register is moved 8-bit positions. Moreover, the characters in the master and slave are effectively exchanged. **Data Register** – Holds data read from passive device, to be sent serially to the SPI Master. **Address Register** – Holds address presented on Address bus. Its contents are incremented every single data portion sent/ received serially through the SPI bus. **SPI Controller** – Detects the beginning and end of SPI transfer. Manages data exchange between DSPIS and a passive device controlled by DSPIS and increments Address Register (SPAD) after any successful transfer.

TRANSFER FORMATS

The software can select any of four combinations of serial clock (SCK) phase and polarity, using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI,

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allows direct interface to almost any existing synchronous serial peripheral.

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Digital multimeters

PERFORMANCE

The following table gives a survey about the Core area and performance in **LATTICE®** devices after Place & Route (all key features included):

Device	Speed grade	LUTs/PFUs	F_{max}
XP	-5	94 / 55	219 MHz
ECP	-5	94 / 55	226 MHz
EC	-5	94 / 55	222 MHz
XP2	-7	69 / 49	306 MHz
ECP2	-7	90 / 55	324 MHz
ECP2M	-7	69 / 49	345 MHz
SC	-7	84 / 55	489 MHz

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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