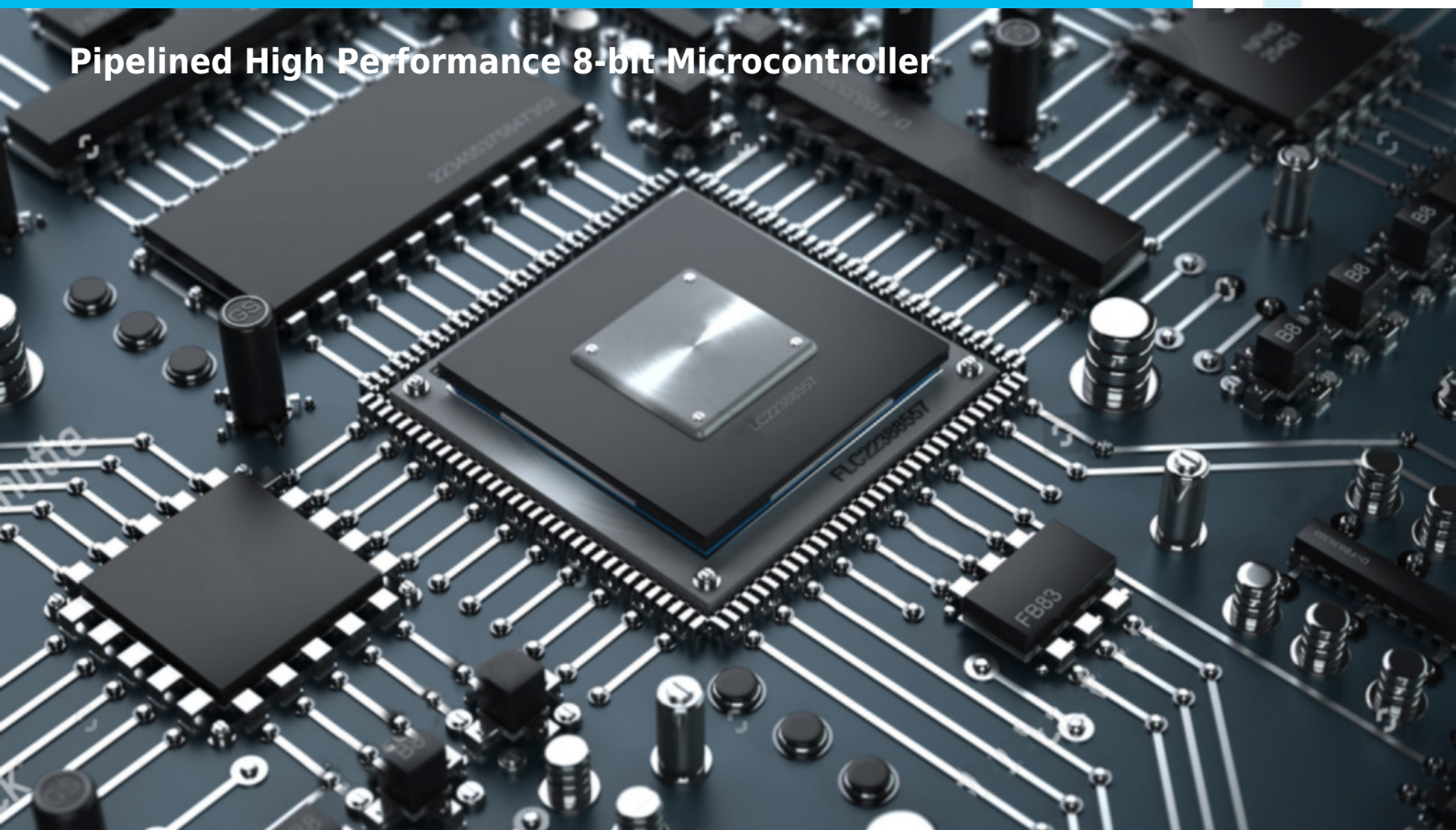
DIGITAL CORE DESIGN

DP80390

Pipelined High Performance 8-bit Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DP80390 8-bit MCU IP Core – High-Performance, Low-Power, Fully Customizable

The **DP80390** is an ultra-high performance, speed-optimized 8-bit softcore MCU designed for both fast on-chip and slower off-chip memory systems. Supporting **up to 8 MB of linear code space** and **16 MB of linear data space**, this softcore is engineered to deliver maximum performance while maintaining an excellent **power-to-performance ratio**, further enhanced by the **advanced Power Management Unit (PMU)**.

Key Features & Configurations:

- **100% 8051 Binary Compatible:** Ensures seamless integration with existing 8051-based software.
- **Flexible Architecture Options:**
  - **Harvard** – separate internal program and data buses for maximum throughput.
  - **Von Neumann** – shared program and external data bus for simplified memory design.
- **Pipelined RISC Design:** Executes **85–200 million instructions per second**, offering **11–15× faster performance** than a standard 80C51 at the same clock frequency.
- **Low-Power Applications:** The core can be clocked **over ten times slower** than the original 8051 without performance loss.

Advanced Peripheral & Debug Support:

- **DoCD™ Real-Time Hardware Debugger:** Non-intrusive debugging of a complete SoC. Supports halting, stepping, running, and memory/register inspection, including internal/external program memories, all SFRs, and user-defined peripherals.
- **Comprehensive Test Bench:** Delivered with a fully automated verification suite for easy integration and validation at all SoC design stages.

Applications: Ideal for **embedded systems, IoT devices, industrial controllers, and any high-performance 8-bit 8051-based SoC requiring low power, extended memory, and advanced debugging capabilities**.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

CPU FEATURES

- Software in 100% compatible with 80390 & 8051 industry standards
  - LARGE mode – 8051 instruction set
  - FLAT mode – 80390 instruction set
- Pipelined RISC architecture enables to run **15.55 times faster,** than the original 80C51 at the same frequency
- **Up to 14.632 VAX MIPS at 100 MHz**
- 24 times faster multiplication
- 12 times faster division
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 8 MB of linear Program Memory
  - 64 kB of internal (on-chip) Program Memory
  - 8 MB external (off-chip) Program Memory
- Up to 16 MB of external (off-chip) Data Memory
- User programmable Program Memory Wait States
- User programmable External Data Memory Wait States
- De-multiplexed Address/Data bus, to allow easy memory connection
- Interface for additional Special Function Registers
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- 2 GHz virtual clock frequency in a 0.25u technological process
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

PROGRAM MEMORY:

The DP80390 soft core is dedicated for operation with Internal and External Program Memory. Its maximum linear size is equal to 8 MB. Internal Program Memory can be implemented as:

– ROM located in address range between 0000h ¸ (ROM_{size}-1)

– RAM located in address range between (64kB-RAM_{size}) ¸ FFFFh

External Program Memory can be implemented as ROM or RAM located in address range between ROM_{size} ¸ 8 MB,

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excluding area occupied by RAM_{size}.

INTERNAL DATA MEMORY:
The DP80390 can address Internal Data Memory of up to 256 bytes The Internal Data Memory can be implemented as Single-Port synchronous RAM.

EXTERNAL DATA MEMORY:
The DP80390 soft core can address up to 16 MB of External Data Memory. Extra DPX (*Data Pointer eXtended*) register is used for segments swapping.

USER SPECIAL FUNCTION REGISTERS:
Up to 104 External (user) Special Function Registers (ESFRs) may be added to the DP80390 design. ESFRs are memory mapped into Direct Memory between addresses 0x80 and 0xFF, in the same manner as core SFRs and may occupy any address that is not occupied by a core SFR.

WAIT STATES SUPPORT:
The DP80390 soft core is dedicated for operation with wide range of Program and Data memories. Slow Program and External Data memory may assert a memory Wait signal to hold up CPU activity.

PERIPHERALS

- **DoCD™ debug unit**
  - Processor execution control
    - Run
    - Halt
    - Step into instruction
    - Skip instruction
  - Read-write all processor contents
    - Program Counter (PC)
    - Program Memory
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Code execution breakpoints
    - up to eight real-time PC breakpoints
    - unlimited number of real-time OPCODE breakpoints
  - Hardware execution watch-point
    - one at Internal (direct) Data Memory
    - one at Special Function Registers (SFRs)
    - one at External Data Memory
  - Hardware watch-points activated at a certain
    - address by any write into memory
    - address by any read from memory
    - address by required data write into memory
    - address by required data read from memory
  - Unlimited number of software watchpoints
    - Internal (direct) Data Memory
    - Special Function Registers (SFRs)
    - External Data Memory
  - Unlimited number of software breakpoints
    - Program Memory(PC)
  - Automatic adjustment of debug data transfer speed rate between HAD and Silicon
  - TTAG or JTAG Communication interface
- **Power Management Unit**
  - Power management mode
  - Switchback feature
  - Stop mode
- **Interrupt Controller**
  - 2 priority levels
  - 2 external interrupt sources
  - 3 interrupt sources from peripherals
- **Four 8-bit I/O Ports**
  - Bit addressable data direction for each line
  - Read/write of single line and 8-bit group
- **Two 16-bit timer/counters**
  - Timers clocked by internal source
  - Auto reload 8-bit timers
  - Externally gated event counters
- **Full-duplex serial port**
  - Synchronous mode, fixed baud rate
  - 8-bit asynchronous mode, fixed baud rate
  - 9-bit asynchronous mode, fixed baud rate
  - 9-bit asynchronous mode, variable baud rate

UNITS SUMMARY

ALU – Arithmetic Logic Unit – performs arithmetic and logic operations during execution of an instruction. Ccontains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.
Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.
Control Unit – Performs the core synchronization and data flow control. This module is directly connected to the Opcode Decoder and manages execution of all microcontroller tasks.
Program Memory Interface – Contains Program Counter (PC) and related logic. Performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C and DoCD™ module.
External Memory Interface – Contains memory access related registers, such as Data Page High (DPH), Data Page Low (DPL) and Data Page Pointer (DPP) registers. Performs external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by the user. This feature is called Program Memory Wait States and it allows core to work with different speed program memories.
Synchronous eXternal Data Memory (SXDM) Interface – Contains XDATA memory access related logic, allowing fast access to synchronous memory devices. Performs the external Data Memory addressing and data transfers. This memory can be used to store large variables frequently accessed by the CPU, improving overall performance of application.
Internal Data Memory Interface – Controls the access into the internal memory of size up to 256 bytes. Contains 8-bit Stack Pointer (SP) register and related logic.
User SFRs Interface – Special Function Registers interface controls the access to special registers. Contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified) by

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using all direct addressing mode instructions.
Interrupt Controller – Responsible for the interrupt manage system of the external and internal interrupt sources. Contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers.
Timers – System timers module. Contains two 16 bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 (or 4) CLK periods when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are sampled every CLK period. It can be used as clock source for UARTs.
UART0 – Universal Asynchronous Receiver and Transmitter module is full duplex – it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of a second byte before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0 reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. The UART0 can be synchronized by Timer 1 or Timer 2 (if present in the system).
Ports – Contains 8051's general purpose I/O ports. Each of the port's pins can be read/written as a single bit or as a 8-bit bus P0, P1, P2, P3.
Power Management Unit – Contains advanced power saving mechanisms with a switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. The switchback feature allows UARTs and interrupts to be processed in a full speed mode, if enabled. It is highly desirable, when the microcontroller is planned to be used in portable and power critical applications.
DoCD™ Debug Unit – A real-time hardware debugger which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DEBUGACS indicate the state of the debugger and CPU. The CODERUN is active when the CPU is executing an instruction. The DEBUGACS pin is active when any access is performed by the **DoCD™** debugger. The **DoCD™** system includes **TTAG** or **JTAG interface** and complete set of tools, to communicate and work with the core in real time debugging. It is built as a scalable unit and some features can be turned off by the user to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to a power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off.

CONFIGURATION

The following parameters of the DP80390 core can be easily adjusted to requirements of a dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Internal Program Memory type: *synchronous / asynchronous*
- Internal Program ROM Memory size: *0 – 64kB*
- Internal Program RAM Memory size: *0 – 64kB*
- Internal Program Memory fixed size: *true / false*
- Interrupts: *subroutines location*
- Power Management Mode: *used / unused*
- Stop mode: *used / unused*
- **DoCD™** debug unit: *used / unused*

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

PERFORMANCE

The following table gives survey about the Core area and performance in **INTEL** Programmable Logic Devices after Place & Route (CPU features and peripherals included):

Device	Speed grade	LE/ALM	F_{max}
STRATIX	-5	2 450	88 MHz
STRATIX-II	-3	1 780 ALUT	159 MHz
STRATIX-III	-2	1 780 ALUT	190 MHz
STRATIX-IV	-2	1 780 ALUT	194 MHz
CYCLONE	-6	2 450	90 MHz
CYCLONE-II	-6	2 450	91 MHz
CYCLONE-III	-6	2 600	110 MHz
Arria GX	-6	1 795 ALUT	111 MHz

Core performance in INTEL FPGA® devices – results given for working system with IDATA, CODE and XDATA memories

For the user, the most important factor is the application speed improvement. The most commonly used arithmetic functions and their improvement are shown in the following table. The improvement was computed as {80C51 clock periods} divided by {DP80390 clock periods} required to execute an identical function. More details are available in the core documentation.

Function	Improvement
8-bit addition (*immediate data*)	**9,00**
8-bit addition (*direct addressing*)	**9,00**
8-bit addition (*indirect addressing*)	**9,00**
8-bit addition (*register addressing*)	**12,00**
8-bit subtraction (*immediate data*)	**9,00**
8-bit subtraction (*direct addressing*)	**9,00**
8-bit subtraction (*indirect addressing*)	**9,00**

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8-bit subtraction (*register addressing*)	**12,00**
8-bit multiplication	**16,00**
8-bit division	**9,60**
16-bit addition	**12,00**
16-bit subtraction	**12,00**
16-bit multiplication	**13,60**
32-bit addition	**12,00**
32-bit subtraction	**12,00**
32-bit multiplication	**12,60**
Average speed improvement:	**11,12**

Dhrystone Benchmark Version 2.1 was used to measure the Core performance. The following table shows DP80390 performance in VAX MIPS per 1 MHz rating.

Device	DMIPS/MHz	Ratio
80C51	0,00941	1,00
DP80390	0,10787	11,46
DP80390+DPTRs	0,13722	14,58
DP80390+DPTRs+SXDM	0,14457	15,36
DP80390+DPTRs+SXDM+MDU32	0,14632	15,55

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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