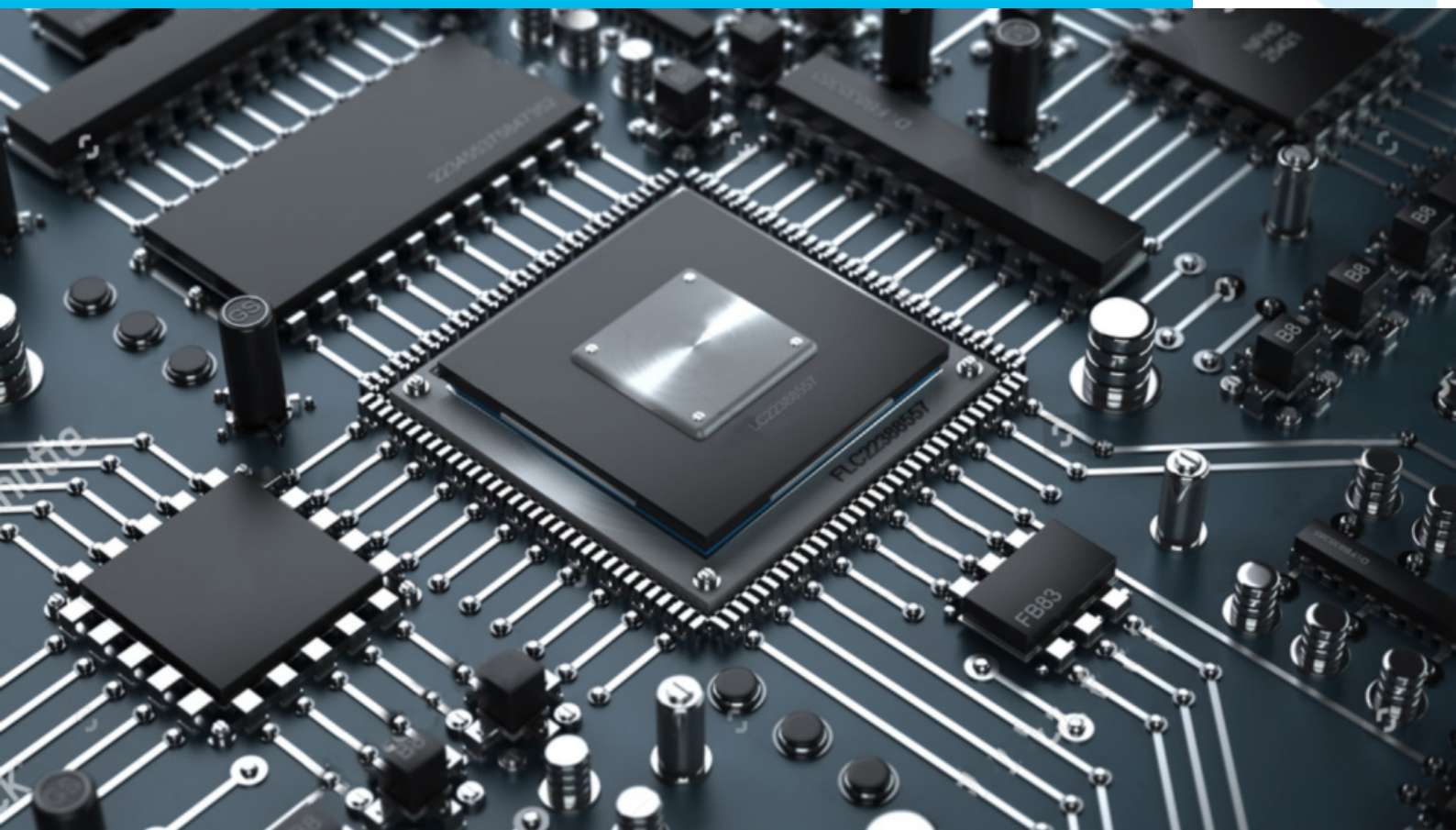
DIGITAL CORE DESIGN

DSPI FIFO



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DSPI_FIFO is a **fully configurable SPI master/slave device**, which allows you to configure polarity and phase of a serial clock signal SCK. It enables a microcontroller to communicate with serial peripheral devices, but also to communicate with an interprocessor in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of information on two independent serial data lines. The **DSPI_FIFO data is simultaneously transmitted and received**. What's more important, this is a technology independent design, which can be easily implemented in variety of process technologies. The DSPI_FIFO system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. **The system can be configured either as a master or slave device** with data rates as high as CLK/4. The clock control logic allows selecting clock polarity and choosing two fundamentally different clocking protocols, to accommodate most available, synchronous serial peripheral devices. When the SPI is configured as a master, the software selects one of eight different bit rates for the serial clock. The DSPI_FIFO automatically drives slave outputs (SS7O – SS0O) selected by the SSCR (**Slave Select Control Register**) and addresses the SPI slave device to exchange serially shifted data. **Error-detection logic is included** to support interprocessor communications. A **write collision detector** indicates when an attempt is made to write data to the serial shift register, while transfer is in progress. A multiple-master mode-fault detector disables DSPI output drivers automatically, if more than one SPI device simultaneously attempts to become a bus master. The DSPI_FIFO supports two DMA modes: single transfer and multi-transfer. These modes allow the DSPI_FIFO to interface to higher performance DMA units, which can interleave their transfers between CPU cycles or execute multiple byte transfers. Our solution is **fully customizable** – it is delivered in the exact configuration to meet your requirements. There is no need to pay extra for unused features and wasted silicon. It includes **fully automated test bench** with **complete set of tests**, allowing easy package validation at each stage of SoC design flow

KEY FEATURES

- **SPI Master**
  - Master and Multi-master operations
  - Two modes of operation: SPI mode and FIFO mode
  - 8 SPI slave select lines
  - System error detection
  - Mode fault error
  - Write collision error
  - Interrupt generation
  - Bit rates generated 1/4 – 1/512 of system clock.
  - Four transfer formats supported
  - Simple interface allows easy connection to microcontrollers
- **SPI Slave**
  - Slave operation
  - Two modes of operation: SPI mode and FIFO mode
  - System error detection
  - Interrupt generation
  - Supports speeds up 1/4 of system clock
  - Simple interface allows easy connection to microcontrollers
  - Four transfer formats supported
- Fully synthesizable
- Two DMA Modes allows single and multi-transfer
- In the FIFO mode transmitter and receiver are each buffered with 16/64 byte FIFO's to reduce the number of interrupts pre-sented to the CPU
- **Optional** FIFO size extension to **128, 256 or 512 Bytes**
- **Available system interface wrappers:**
  - **AMBA – APB Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready

UNITS SUMMARY

Shift register and Read Data Buffer – a central element in the SPI system. The system is single buffered in the transmit direction and double buffered in the receive direction. It means that new data for transmission cannot be written to the shifter, until the previous transaction is complete; however, received data is transferred into a parallel read data buffer, so the shifter is free to accept a second serial character. As long as the first character is read out of the read data buffer before the next serial character is ready to be transferred, no overrun condition will occur. When an SPI transfer occurs, an 8-bit character is shifted out on data pin, while a different 8-bit character is simultaneously shifted in a second data pin. Another way to view this transfer is that an 8-bit shift register in the master and another 8-bit shift register in the slave is connected as a circular 16-bit shift register. When the transfer occurs, this distributed shift register is shifted eight bit positions; thus, the characters in master and slave are effectively exchanged.
Receiver FIFO – The Rx FIFO can be 64 (128, 256, 512) levels deep, it receives data until the number of bytes in the FIFO, equals the selected interrupt trigger level. At that time, if interrupt is enabled, the DSPI_FIFO will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it is full, and will not accept any next byte. Any more data entering the Rx shift register will set the Over-run Error flag.
Transmitter FIFO – The Tx portion of the DSPI_FIFO

transmits data through SO/MO, as soon as the CPU loads a byte into the Tx FIFO in Master mode. In Slave mode, the transmission is started after correct edge of the SCK signal. The DSPI_FIFO will prevent loads to the Tx FIFO, if it currently holds 64 (128, 256, 512) characters (depending on SFCR [5] bit value and selected FIFO size). Loading to the Tx FIFO again will be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

Control Register may be read or written at any time, it is used to configure the DSPI_FIFO System. This register controls the mode of transmission (Master, Slave), polarity and phase of SPI Clock and transmission speed.

Status Register (SPSR) contains flags, indicating the completion of transfer or occurrence of system errors. All flags are set automatically when the corresponding event occur and cleared by software sequence.

Slave Select Control Register configures which slave select output should be driven while SPI master transfer. Contents of SSCR register is automatically assigned on SS7O-SS0O pins when DSPI master transmission starts.

SPI Clock Logic – Software can select any from four combinations of serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow master device communication with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI allows direct interface to almost any existing synchronous serial peripheral.

SPI Controller – The SPI Controller manages Master/Slave operation and controls the transmission. It also manages the transmission speed and format (Phase and polarity). Controller itself generates interrupt request and selects transmission errors.

TRANSFER FORMATS

The software can select any of four combinations of serial clock (SCK) phase and polarity, using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical, for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow a master device to communicate with peripheral slaves, having different requirements. The flexibility of the SPI system on the DSPI allow direct interface to almost any existing synchronous serial peripheral.

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Digital multimeters

PERFORMANCE

The following table gives a survey about the Core area and performance in **XILINX®** devices after Place & Route:

Device	LUTs/Slices	Memory Blocks	F_{max} MHz
ZYNQ 7000	292	1	330
ZYNQ	338/158	2	215
KINTEX Ultra Scale	279	1	330
KINTEX 7	332/186	2	264
ARTIX 7	341/193	2	266
VIRTEX Ultra Scale	279	1	330
VIRTEX 7	332/163	2	336
VIRTEX 6	303/152	2	216
VIRTEX 5	351/167	2	222
VIRTEX 4	458/290	2	212
SPARTAN 6	330/122	2	162
SPARTAN 3E	451/286	2	129
SPARTAN 3	468/293	2	138

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

LICENSING

Transparent and clearly defined licensing methods without royalty-per-chip fees, make use of our IP Cores easy & simple.
– ***Single-Site license option*** – dedicated to small and middle sized companies, which run their business in one place.
– ***Multi-Site license option*** – dedicated to corporate customers who operate at several locations. The licensed product can be used in selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.
There are two formats of the delivered IP Core:
– VHDL or Verilog RTL synthesizable HDL Source code
– FPGA EDIF/NGO/NGD/QXP/VQM Netlist

CONTACT

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