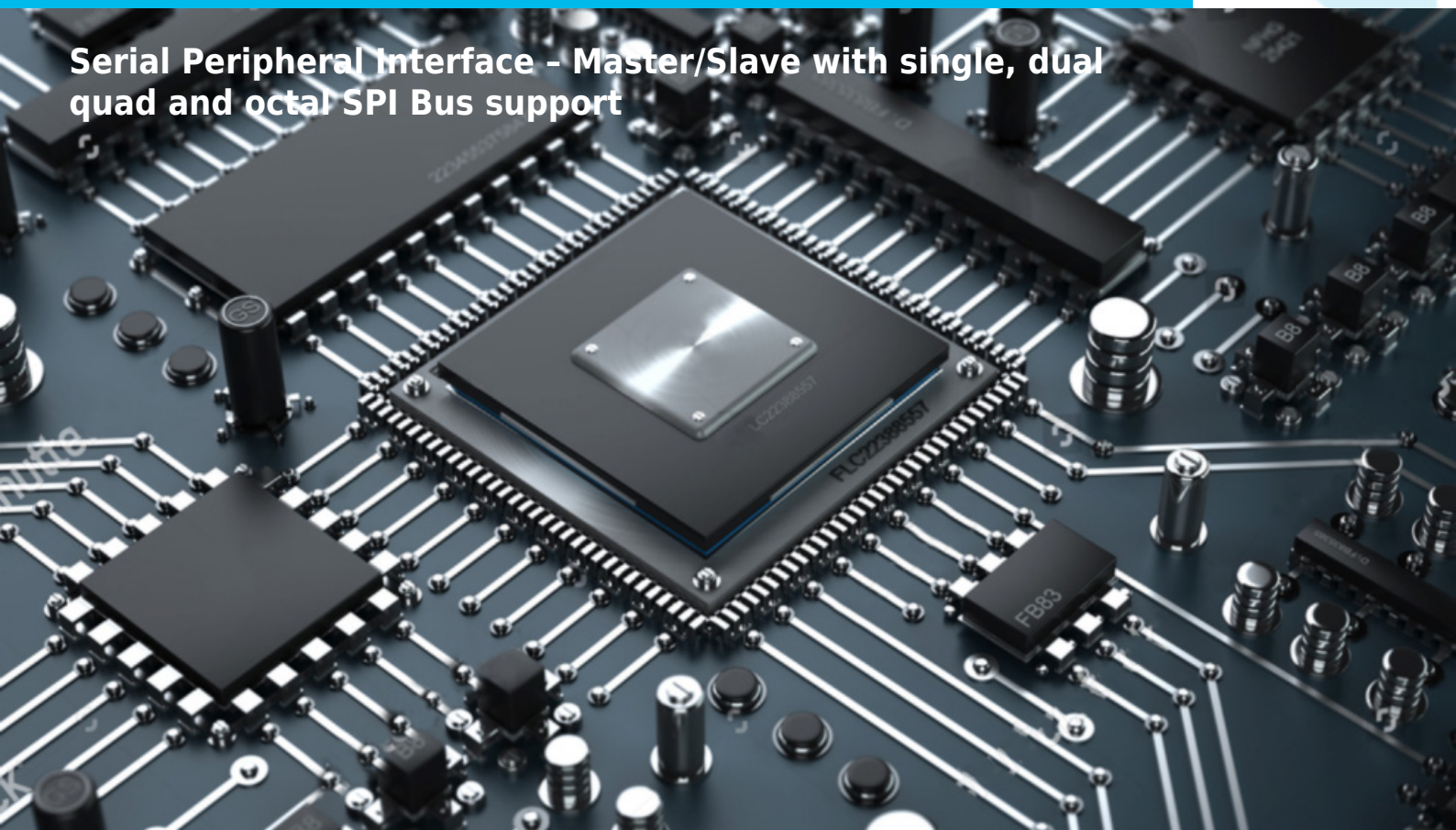
DIGITAL CORE DESIGN

DQSPI

Serial Peripheral Interface – Master/Slave with single, dual quad and octal SPI Bus support



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DQSPI – High-Performance Quad SPI IP Core for APB, AHB, and AXI Designs

The **DQSPI** is a **revolutionary Quad SPI IP Core** engineered for design teams who demand **maximum throughput**, **low latency**, and **flexible integration**. Fully compatible with **APB, AHB, and AXI buses**, it delivers one of the fastest serial memory interfaces available for both **SoC** and **FPGA** designs.

Supporting **Single, Dual, and Quad SPI** modes with **Double Data Rate (DDR)** operation, the DQSPI enables **8 bits of data per SCK cycle**, making it ideal for systems requiring **high-speed code execution**, **fast memory access**, or **real-time data streaming**.

Engineered for Modern Embedded Systems

The DQSPI interfaces seamlessly with **all 8-, 16-, and 32-bit processors**, regardless of endianness. Its flexible architecture supports standard SPI peripherals from multiple vendors, which makes it an excellent choice for new designs and drop-in replacements.

Typical use cases include:

- high-speed Quad SPI flash memories
- real-time data logging
- inter-processor communication
- Execute-In-Place (XiP) architectures
- low-pin-count, high-performance embedded systems

Key Performance Features

Blazing-Fast Transfers

- Supports **Single, Dual, and Quad SPI**
- **DDR protocol** doubles bandwidth
- Achieves **data rates up to CLK/2** (vs. typical vendor limit of CLK/8)
- Ideal for high-performance SoCs and FPGAs

Advanced Clock Control

- Programmable clock **polarity**, **phase**, and **four clocking protocols**
- Supports a wide variety of synchronous serial peripherals
- Precisely tuned for embedded applications with tight timing budgets

Master/Slave Configurable

The DQSPI can operate as a **master** or **slave**, enabling seamless integration into:

- multi-master systems
- shared bus environments
- communication between processors or controllers

Robust Reliability and Error Handling

To support demanding applications, the DQSPI includes advanced safety and reliability mechanisms:

- **Write-collision detection**
- **Multiple-master mode fault detection**
- Automatic disable of drivers under conflict
- Error-reporting logic for inter-processor communication

These features make the DQSPI highly reliable in automotive, industrial, and mission-critical embedded environments.

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DMA Support for Maximum Throughput

The IP Core supports **two independent DMA modes**:

- **Single-transfer mode**
- **Multi-transfer mode**

This allows high-performance DMA units to interleave transfers with CPU cycles or perform burst data transfers without processor overhead.

Technology-Independent Design

Like all DCD-SEMI solutions, the DQSPI is:

- **fully synthesizable**
- **portable across semiconductor technologies**
- ready for **ASIC, SoC, and FPGA** implementation

This ensures long-term product scalability and easy migration across multiple platforms.

Fully Customizable IP Core

The DQSPI is delivered in a configuration tailored to your design requirements:

- width of data paths
- clocking scheme
- DMA options
- master/slave configuration
- peripheral compatibility

Our team customizes the DQSPI to minimize your integration effort and accelerate time-to-market.

Why Design Engineers Choose DQSPI

✔ Ultra-fast Quad SPI + DDR performance
✔ Compatible with APB, AHB, and AXI bus structures
✔ Supports any 8/16/32-bit CPU architecture
✔ XiP-ready for instant code execution from external flash
✔ Superior data rate (CLK/2 vs typical CLK/8)
✔ Robust error detection and multi-master support
✔ Fully configurable and technology-independent

Watch the DQSPI presentation on DCD's YouTube:

As Seen On YouTube

Which One to Choose DQSPI vs DOSPI

Feature / Requirement	DQSPI (Quad SPI)	DOSPI (Octal SPI)	Which to choose?
Bus Width	1-bit (Single), 2-bit (Dual), 4-bit (Quad)	1-bit, 2-bit, 4-bit, **8-bit (Octal)**	If you need **max throughput**, choose **DOSPI**.
Max Data Throughput	Up to **8 bits per SCK** (Quad + DDR)	Up to **16 bits per SCK** (Octal + DDR)	DOSPI for high-bandwidth memory boot or XIP; DQSPI is optimal for mid-range.
Supported Protocols	Single, Dual, Quad SPI	Single, Dual, Quad, **Octal SPI**	DOSPI covers everything DQSPI does — and more.
DDR Support (Double Data Rate)	Yes (Dual & Quad)	Yes (Dual, Quad & Octal)	Both excellent for speed-critical systems.
Supported CPU Bus Widths	8 / 16 / 32-bit	8 / 16 / 32-bit	Both match common MCU/SoC designs.
Clocking Flexibility	Full control of SCK polarity, phase & protocols	Full control of SCK polarity, phase & protocols	Equal – both adaptable to any SPI memory.
Typical Use Cases	Quad-SPI NOR/NAND, XIP boot, mid-range SoCs	Octal-SPI NOR/NAND, ultra-fast XIP, high-end SoCs, performance-critical systems	Choose DQSPI for cost-optimized designs; DOSPI for high-end devices.
Interprocessor Communication	Yes	Yes	Same functionality.
DMA Support	Single & multi-transfer modes	Single & multi-transfer modes	Same — both integrate with high-performance DMA.
Master/Slave Mode	Both supported	Both supported	Same.
Performance Advantage	Data rate up to **CLK/2**	Data rate up to **CLK/2** (vs typical market CLK/8)	Both outperform competitors; DOSPI achieves highest bandwidth.
Best Match For	Mid-range embedded systems, cost-sensitive devices, Quad-SPI flash	High-performance designs, fast booting, real-time apps, Octal flash	Engineers optimize cost → DQSPI, optimize speed → DOSPI.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

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DCD-SEMI SPI IP Cores

	DSPI	DQSPI	DOSPI	DFSPI	DOSPIS	DESPI	DESPIS
SPI mode	SINGLE	SINGLE, DUAL, QUAD	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD, OCTAL	SINGLE, DUAL, QUAD	SINGLE, DUAL, QUAD
Operation mode	Master only	Master only	Master only	Master only	Slave only	Master only	Slave only
Data rate	Low	Middle	High	High	High	Middle	Middle
Cost / complexity	Low	Middle	Middle	High	Middle	High	High
XIP support	Optional	Optional	Optional	Yes	No	No	No
DDR support	Yes	Yes	Yes	Yes	No	No	No
Standard supported	xSPI partially	xSPI partially	xSPI partially	xSPI, HyperBus, XCELLA	xSPI partially	Intel eSPI 1.6	Intel eSPI 1.6
Best option for	Memory controller, SPI peripheral controller i.e. sensors	Memory controller, SPI peripheral controller i.e. sensors	Memory controller, SPI peripheral controller i.e. sensors	Memory controller (Flash, DRAM, PSRAM, HyperRAM and other), program code execution	Serial bus to parallel bus bridge, RAM connection to SPI interface	PC mother-boards	PC mother-boards

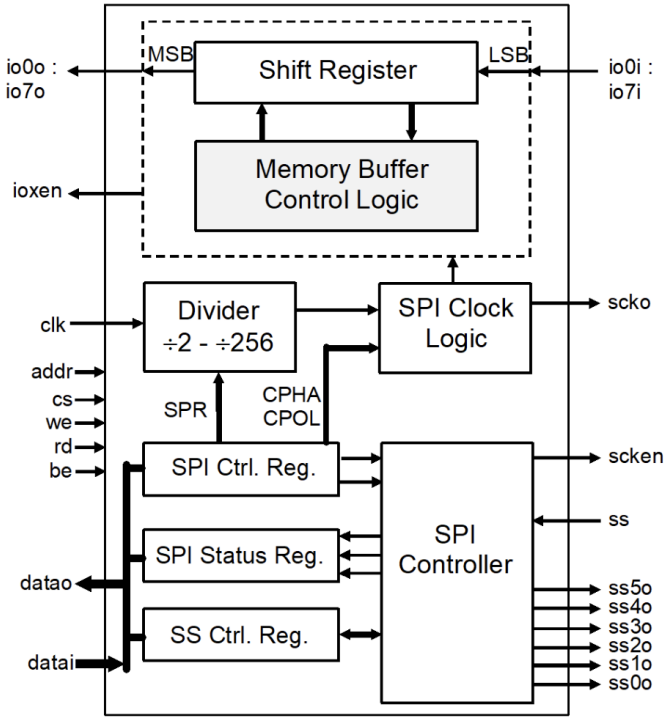
KEY FEATURES

- Operates with 8, 16 and 32 bit CPUs
- Full duplex synchronous serial data transfer
- DMA support
- Support for 32, 16 and 8 bit systems
- Support for various system Bus Standards
- Single, Dual, Quad and Octal SPI transfer
- DDR support (Double Data Rate)
- Optionally available Execute-in-Place
- Multimaster system supported
- Optional FIFO size extension (128, 256, 512B)
- Up to 7 SPI slaves can be addressed (more Slave Select Outputs can be added upon request)
  - Software Slave Select Output – SSO - selection
  - Automatic Slave Select outputs assertion during each byte transfer
- System error detection
- Interrupt generation
- Various Bit rates supported
- Bit rate in fast SPI Mode ½ CLK
- Four transfer formats
- Simple CPU and DMA interface
- Fully synthesizable, static synchronous de-sign with no internal tri-states

UNIT SUMMARY

Shift Register – The heart of the DSPI controller, shifts in and out data from the DSPI controller regarding to the appropriate edge of the SCK.
Receiver FIFO - The Rx FIFO can be 64 (128, 256, 512) levels deep, it receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if interrupt is enabled, the DSPI will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it is full, and will not accept any next byte. Any more data entering the Rx shift register will set the Overrun Error flag.
Transmitter FIFO - the Tx portion of the DSPI transmits data through SO/MO as soon as the CPU loads a byte into the Tx FIFO in Master mode. In Slave mode the transmission is started after correct edge of the SCK signal. The DSPI will prevent loads to the Tx FIFO if it currently holds 64 (128, 256, 512) characters (depending on SFCR(5) bit value and selected FIFO size). Loading to the Tx FIFO again will be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.
Divider – Divider allows dividing the global CLK signal by 2 up to 1024. This divided signal is used to generate the SCKO – Serial Clock Signal in Master mode.
SPI Clock Logic, - this module controls phase and polarity of generated/received SCK signal. On correct SCK edge generates shift signal to SPI Shift register.
SPI Controller - controls Master/Slave operations, manages the interrupt requests, error detection etc.

BLOCK DIAGRAM



PERFORMANCE

The following table gives a survey about the Core performance in **INTEL FPGA** devices after Place & Route (all key features included):

Device	Speed grade	LE/ALM	Memory Bits	F_{max}
ARIA GX	-6	287/201	1 024	158 MHz
ARIA 10	-1	371	1 024	327 MHz
CYCLONE	-6	382	1 024	152 MHz
CYCLONE2	-6	387	1 024	186 MHz
CYCLONE3	-6	375/200	1 024	234 MHz
CYCLONE4	-6	375/200	1 024	217 MHz

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CYCLONE5	-6	288/200	1 024	187 MHz
MAX 10	-6	633	1 024	133 MHz
STRATIX	-5	382	1 024	167 MHz
STRATIX2	-3	289	1 024	314 MHz
STRATIX3	-2	300/242	1 024	408 MHz
STRATIX4	-2	290/240	1 024	360 MHz
STRATIX5	-2	307/212	1 024	375 MHz
STRATIX GX	-5	382	1 024	180 MHz
STRATIX2 GX	-3	288/201	1 024	254 MHz

TRANSFER FORMATS

The software can select any of four combinations of serial clock (SCK) phase and polarity, using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit, selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI allows direct interface to almost any existing synchronous serial peripheral.

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Digital multimeters

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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