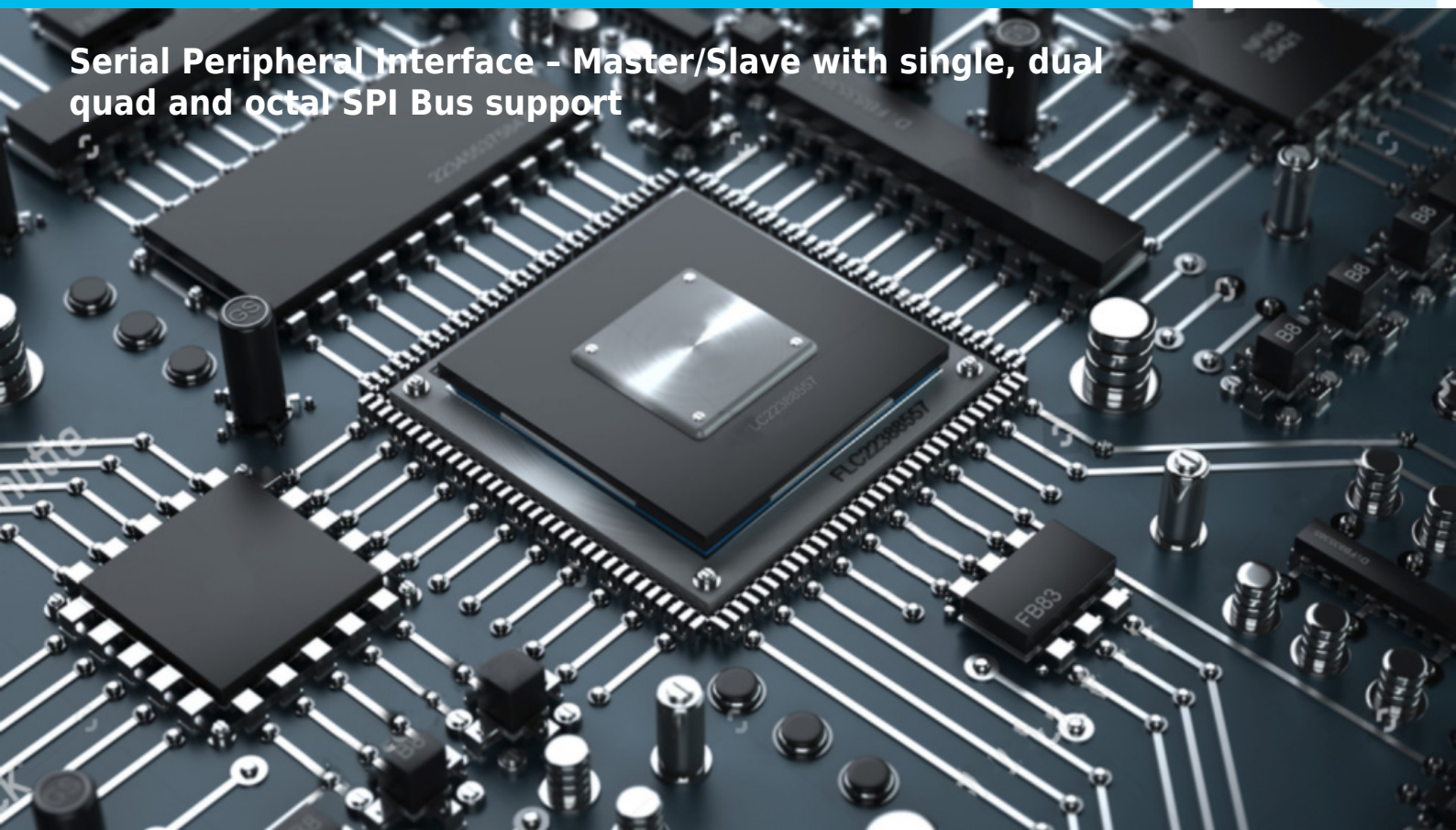
DIGITAL CORE DESIGN

DQSPI

Serial Peripheral Interface – Master/Slave with single, dual quad and octal SPI Bus support



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DQSPI bridge to APB, AHB, and AXI bus, it is a revolutionary quad SPI designed to offer **the fastest operations available for any serial SPI memory**. It is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Moreover, the IP Core **supports all 8, 16, 32-bit processors** available on the market. The DQSPI is a fully configurable SPI master/slave device, which allows you to configure the polarity and phase of serial clock signal SCK. It enables the microcontroller to communicate with **fast serial SPI memories** and **serial peripheral devices**. Moreover, it's capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes the shifting and sampling of information on four serial data lines. In the **Single** SPI mode, data is simultaneously transmitted and received, while in **DUAL**, and **QUAD** SPI modes, data is shifted in or out respectively on two and four data lines at once. Additionally, transfer speed can be doubled by using the **DDR protocol** (Double Data Rate) – This feature allows the DQSPI to transfer/receive data on both falling and rising edges of SCK. The DDR together with QUAD SPI transfer allows 8 bits of data to be sent/received within a single SCK clock cycle. This makes the DQSPI perfect for systems, where performance is essential, or where the code can be moved from non-volatile memory to fast RAM, or for systems where device size and cost are the keys, or where the program code can be executed directly from non-volatile memory, using an approach known as **Execute-in-Place**. DCD's IP Core is a **technology-independent** design that can be implemented in variety of process technologies. The DQSPI system is flexible enough to **interface directly with numerous standard product peripherals from several manufacturers**. The system can be configured as a master or slave device. **Data rates are as high as CLK/2**, when other vendors' solutions offer just CLK/8. Clock control logic allows selecting clock polarity, phase and four fundamentally different clocking protocols, to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, the software selects bit rates for the serial clock. The DQSPI automatically drives selected by SSCR (Slave Select Control Register) slave select outputs (SS7O – SS0O), and addresses the SPI slave device to exchange serially shifted data. **Error detection logic** is included, to support interprocessor communications. A **write collision detector** indicates when an attempt is made to write data to the serial shift register, while the transfer is in progress. A **multiple-master mode fault detector** disables DQSPI output drivers automatically if more than one SPI device simultaneously attempts to become a bus master. The **DQSPI supports two DMA modes: single transfer and multi transfer**. These modes allow the DQSPI to interface to higher performance DMA units which can interleave their transfers between CPU cycles or execute multiple byte transfers. The DQSPI is fully customizable – it is delivered in the exact configuration to meet your requirements.

Watch the DQSPI presentation on DCD's YouTube:

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.

- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

KEY FEATURES

- Operates with 8, 16 and 32 bit CPUs
- Full duplex synchronous serial data transfer
- DMA support
- Support for 32, 16 and 8 bit systems
- Support for various system Bus Standards
- Single, Dual, Quad and Octal SPI transfer
- DDR support (Double Data Rate)
- Optionally available Execute-in-Place
- Multimaster system supported
- Optional FIFO size extension (128, 256, 512B)
- Up to 7 SPI slaves can be addressed (more Slave Select Outputs can be added upon request)
  - Software Slave Select Output – SSO - selection
  - Automatic Slave Select outputs assertion during each byte transfer
- System error detection
- Interrupt generation
- Various Bit rates supported
- Bit rate in fast SPI Mode ½ CLK
- Four transfer formats
- Simple SPU and DMA interface
- Fully synthesizable, static synchronous de-sign with no internal tri-states
- **Available system interface wrappers:**

- **AMBA – APB / AHB / AXI Bus**
- **Altera Avalon Bus**
- **Xilinx OPB Bus**

UNIT SUMMARY

Shift Register – The heart of the DSPI controller, shifts in and out data from the DSPI controller regarding to the appropriate edge of the SCK.
Receiver FIFO - The Rx FIFO can be 64 (128, 256, 512) levels deep, it receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if interrupt is enabled, the DSPI will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it is full, and will not accept any next byte. Any more data entering the Rx shift register will set the Overrun Error flag.
Transmitter FIFO - the Tx portion of the DSPI transmits data through SO/MO as soon as the CPU loads a byte into the Tx FIFO in Master mode. In Slave mode the transmission is started after correct edge of the SCK signal. The DSPI will prevent loads to the Tx FIFO if it currently holds 64 (128, 256, 512) characters (depending on SFCR(5) bit value and selected FIFO size). Loading to the Tx FIFO again will be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.
Divider – Divider allows dividing the global CLK signal by 2 up to 1024. This divided signal is used to generate the SCKO – Serial Clock Signal in Master mode.
SPI Clock Logic, - this module controls phase and polarity of generated/received SCK signal. On correct SCK edge generates shift signal to SPI Shift register.
SPI Controller - controls Master/Slave operations, manages the interrupt requests, error detection etc.

TRANSFER FORMATS

The software can select any of four combinations of serial clock (SCK) phase and polarity, using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit, selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers, to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the DSPI allows direct interface to almost any existing synchronous serial peripheral.

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APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Digital multimeters

PERFORMANCE

The following table gives a survey about the Core performance in **INTEL FPGA®** devices after Place & Route (all key features included):

Device	Speed grade	LE/ALM	Memory Bits	F_{max}
ARIA GX	-6	287/201	1 024	158 MHz
ARIA 10	-1	371	1 024	327 MHz
CYCLONE	-6	382	1 024	152 MHz
CYCLONE2	-6	387	1 024	186 MHz
CYCLONE3	-6	375/200	1 024	234 MHz
CYCLONE4	-6	375/200	1 024	217 MHz
CYCLONE5	-6	288/200	1 024	187 MHz
MAX 10	-6	633	1 024	133 MHz
STRATIX	-5	382	1 024	167 MHz
STRATIX2	-3	289	1 024	314 MHz
STRATIX3	-2	300/242	1 024	408 MHz
STRATIX4	-2	290/240	1 024	360 MHz
STRATIX5	-2	307/212	1 024	375 MHz
STRATIX GX	-5	382	1 024	180 MHz
STRATIX2 GX	-3	288/201	1 024	254 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application

- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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