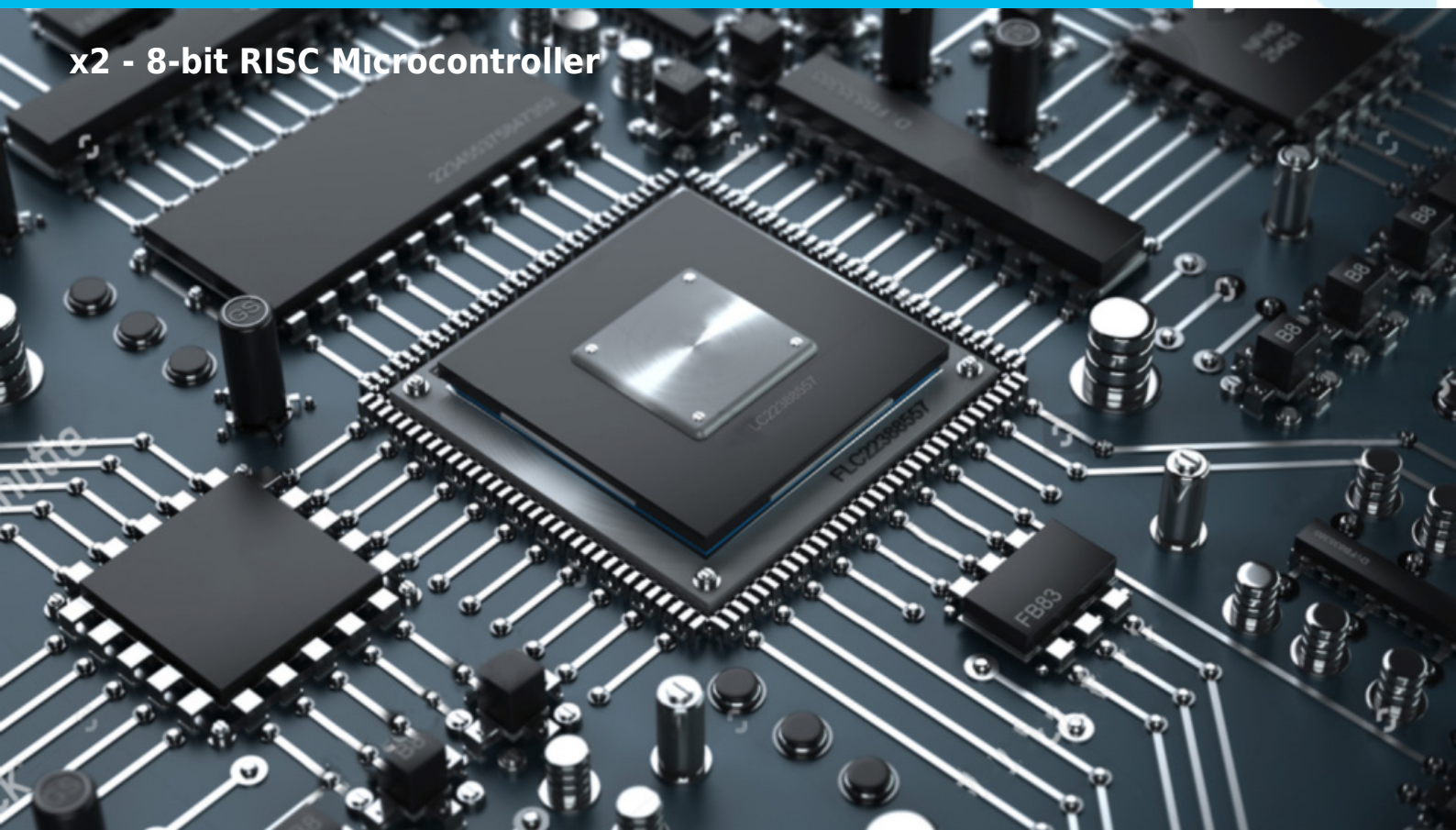
DIGITAL CORE DESIGN

DFPIC1655X

x2 - 8-bit RISC Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DFPIC1655X 8-bit PIC Microcontroller IP Core – High-Performance, Low-Power, Fully Static

The **DFPIC1655X** is a **low-cost, high-performance, 8-bit, fully static soft IP Core**, designed to operate with fast memory while optimizing **power consumption and performance**. Fully **software-compatible with industry-standard PIC 16XXX microcontrollers**, it features a **modified RISC architecture** delivering up to **2× higher performance** than the original implementation.

The core provides enhanced capabilities, including a **configurable hardware stack** and **multiple internal and external interrupt sources**. Its **Harvard architecture** separates instruction and data buses, supporting **14-bit wide instructions** and 8-bit data operations. A **power-down SLEEP mode** allows significant energy savings, with wake-up triggered via external or internal interrupts and resets. An integrated **Watchdog Timer (WDT)** with a dedicated clock ensures protection against software lock-ups.

Ideal for a wide range of applications, the DFPIC1655X is perfect for **high-speed automotive and appliance motor control**, **low-power remote transmitters/receivers**, **pointing devices**, and **telecom processors**. Its small footprint and **power-saving features** make it an excellent solution for **embedded systems with area and energy constraints**.

The DFPIC1655X is delivered **fully customizable**, in an exact configuration to meet project requirements, with no unnecessary features or wasted silicon. It includes a **fully automated test bench and verification suite**, simplifying SoC integration and validation.

Built-in support for **DCD's proprietary DoCD™ hardware debugger** enables **real-time, non-intrusive debugging** of the entire SoC. Developers can halt, run, step into, or skip instructions, and read/write all microcontroller contents, including registers, SFRs, program memory, data memory, and user-defined peripherals.

Applications: Automotive motor control, industrial embedded systems, battery-powered devices, low-power telecom applications, remote monitoring, pointing devices.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

CPU FEATURES

- Software compatible with PIC16C55X industry standard
- Harvard RISC architecture
  - **2 times faster comparing to the original implementation**
- 35 instructions
- 14 bit wide instruction word
- **Up to 32 kB of internal Data Memory**
- **Up to 64K bytes of Program Memory**
- Configurable hardware stack
- Power saving SLEEP mode
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- Technology independent HDL Source Code
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

PERIPHERALS

- **Two 8 bit I/O ports**
  - *Four 8-bit corresponding TRIS registers*
  - *Interrupt feature on PORTB(7:4) change*
- **Timer 0**
  - *8-bit timer/counter*
  - *Readable and Writable*
  - *8-bit software programmable prescaler*
  - *Internal or external clock select*
  - *Interrupt generation on timer overflow*
  - *Edge select for external clock*
- **Watchdog Timer**
  - *Configurable Time out period*
  - *7-bit software programmable prescaler*
  - *Dedicated independent Watchdog Clock input*
- **Interrupt Controller**
  - *Three individually maskable Interrupt sources*
    - *External interrupt INT*
    - *Timer Overflow interrupt*
    - *Port B[7:4] change interrupt*
- **DoCD™ debug unit**
  - *Processor execution control*
    - *Run*
    - *Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
    - *Hardware Stack and Stack Pointer*
  - *Hardware execution breakpoints*
    - *Program Memory*

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- *Data Memory*
- *Special Function Registers (SFRs)*
- *Three wire communication interface*

OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented DFPIC1655X Microcontroller Core) are also available. The optional peripherals can be implemented upon customer's request.

- **Full duplex UART**
- **SPI – Master and Slave Serial Peripheral Interface**
- **PWM – Pulse Width Modulation Timer**
- **I2C bus controller – Master**
- **I2C bus controller – Slave**
- **READY signal to for operation with slow program and data memories.**

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs arithmetic and logic operations, during execution of an instruction. This module contains work register (W) and Status register.
Control Unit – It performs the core synchronization and data flow control. This module manages execution of all instructions. Performs decode and control functions for all other blocks. It contains program counter (PC) and hardware stack.
Hardware Stack – it's a configurable hardware stack. The stack space is neither part of program nor data space and the stack pointer is not readable or writable. The PC is pushed onto the stack, when CALL instruction is executed or an interrupt causes a branch. The stack is popped, during RETURN, RETFIE and RETLW instruction execution. The stack operates as a circular buffer. This means that after the stack has been pushed eight times, the ninth push overwrites the value, which was stored from the first push.
RAM Controller – It performs interface functions between Data Memory and DFPIC1655X internal logic. It assures correct Data memory addressing and data transfers. The DFPIC1655X supports two addressing modes: direct or indirect. In Direct Addressing the 9-bit direct address is computed from RP(1:0) bits (STATUS) and 7 least significant bits of instruction word.
Indirect addressing is possible, by using the INDF register. Any instruction using INDF register actually accesses data pointed to, by the file select register – FSR. Reading INDF register indirectly, will produce 00h. Writing to the INDF register indirectly, results in a no-operation. An effective 9-bit address is obtained by concatenating the IRP bit (STATUS) and the 8-bit FSR register.
Interrupt Controller – Interrupt Controller module is responsible for interrupt manage system, for the external and internal interrupt sources. It contains interrupt related register, called INTCON. The DFPIC1655X has three interrupt sources:

- External interrupt INT
- TMR0 overflow interrupt
- PORTB change interrupt (pins B7:B4)

The interrupt control register INTCON records individual interrupt requests in flag bits. A global interrupt enable bit, GIE enables all unmasked interrupts. Each interrupt source has an individual enable bit, which can enable or disable corresponding interrupt. When an interrupt is responded to, the GIE is cleared, to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. The interrupt flag bits must be cleared in software, before re-enabling interrupts.
Timer 0 – Main system's timer and prescaler. This timer operates in two modes: 8-bit timer or 8-bit counter. In the "timer mode", timer registers are incremented every 4 CLK periods. When the prescaler is assigned into the TIMER, pre-scale ratio can be divided by 2, 4 .. 256. In the "counter mode", the timer register is incremented every falling or rising edge of T0CKI pin, depending on T0SE bit in OPTION register.
Watchdog Timer– it's a free running timer. WDT has its own clock input, separate from system clock. It means, that the WDT will run, even if the system clock is stopped by execution of SLEEP instruction. During normal operation, a WDT time-out generates a Watchdog reset. If the device is in SLEEP mode, the WDT time-out causes the device to wake up and continue with normal operation.
I/O Ports – Block contains DFPIC1655X's general purpose I/O ports and data direction registers (TRIS). The DFPIC1655X has two 8-bit full bi-directional ports PORT A, PORT B. Read and write accesses to the I/O port are performed via their corresponding SFR's PORTA, PORTB. The reading instruction always reads the status of Port pins. Writing instructions always write into the Port latches. Each port's pin has an corresponding bit in TRISA and TRISB registers. When the bit of TRIS register is set, this means, that the corresponding bit of port is configured as an input (output drivers are set into the High Impedance).
DoCD™ – Debug Unit – it's a real-time hardware debugger, providing debugging capability of a whole SoC system. Unlike other on-chip debuggers **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal, external, program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

IMPROVEMENT

Most instructions of the DFPIC1655X are executed within 2 CLK cycles, except the conditional program memory branches

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in case when the condition of branch instruction is met. The following table shows sample instructions execution times.

Mnemonic operands	DFPIC1655X (CLK cycles)	PIC16C554 (CLK cycles)	Impr.
ADDWF	2	4	2
ANDWF	2	4	2
RLF	2	4	2
BCF	2	4	2
DECFSZ	2(4)[1]	4(8)[1]	2
INCFSZ	2(4)[1]	4(8)[1]	2
BTFSC	2(4)[1]	4(8)[1]	2
BTFSS	2(4)[1]	4(8)[1]	2
CALL	2	8	4
GOTO	2	8	4
RETFIE	2	8	4
RETLW	2	8	4
RETURN	2	8	4

1 number of clock in case that result of operation is 0.

PERFORMANCE

The following table gives a survey about the Core area and performance in **LATTICE FPGA** devices after Place & Route:

Device	Speed grade	LUTs/PFU	F_{max}
XP	-5	757/203	57 MHz
ECP	-5	757/203	62 MHz
EC	-5	757/203	62 MHz

*CPU – consisted of ALU, Control Unit, Bus Controller, Hardware Stack, External INT pin Interrupt Controller, Extended interrupt controller, 512 B RAM, 8k of Program memory

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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