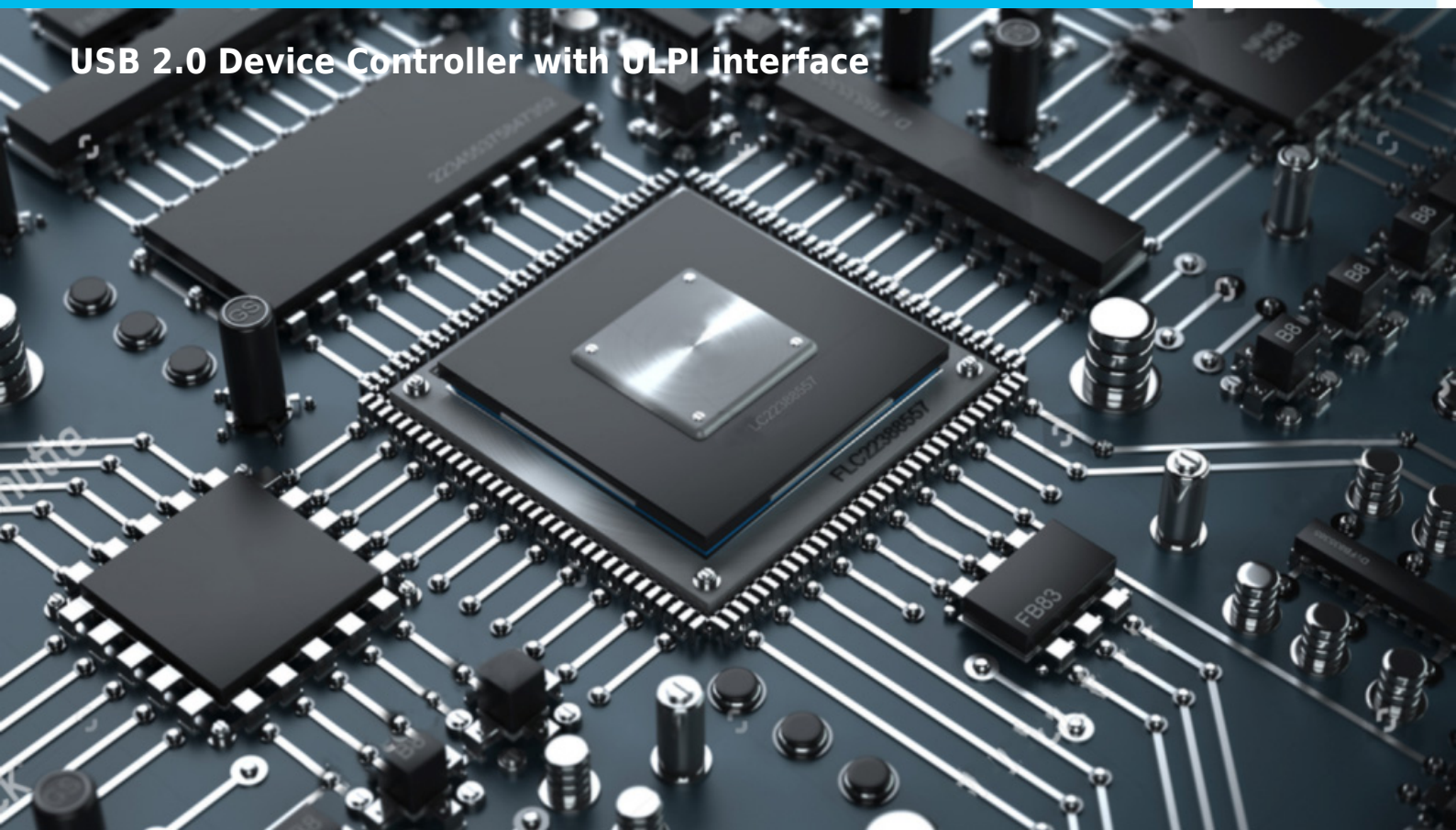
DIGITAL CORE DESIGN

DUSB2-ULPI

USB 2.0 Device Controller with ULPI interface



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DUSB2-ULPI bridge to APB, AHB, AXI bus, it is a hardware implementation of a full/high-speed peripheral controller that interfaces to an **ULPI bus transceiver**. The DUSB2-ULPI contains a USB PID and address recognition logic, as well as state machines, to handle USB packets and transactions, endpoints number recognition logic and endpoints FIFO control logic. The DUSB2-ULPI is designed to **support:**

- **12 Mb/s "Full Speed" (FS),**
- **480 Mb/s "High Speed" (HS)**.

The design is **technology independent** and thus can be implemented in variety of process technologies. This core **strictly conforms to the USB Specification v2.0 and ULPI v2.0**. It is **delivered with fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of SoC design flow.

KEY FEATURES

- Full compliance with the USB 2.0 specification
- Full-speed 12 Mbps operation
- High-speed 480 Mbps operation
- Software configurable EP0 control endpoint size 8-64 bytes
- Software configurable 15 IN/OUT endpoints:
  - configurable number of endpoints
  - configurable type of each endpoint: INTERRUPT, BULK or ISOCHRONOUS
  - configurable direction of each endpoint
  - configurable size of each endpoint: 8-1024 bytes
- Supports ULPI Transceiver Macrocell Interface
- Synchronous RAM interface for FIFOs
- Suspend and resume power management functions
- Simple interface allows easy connection to the 8-, 16-, 32-bit CPUs
- Allows operation from a wide range of CPU clock frequencies
- Fully synthesizable
- Static synchronous design
- Positive edge clocking
- No internal tri-states
- Scan test ready
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

UNITS SUMMARY

ULPI Interface – The ULPI interface is clocked by ULPICLK clock @60MHz and manages communication with USB 2.0 Transceiver Macrocell. It is responsible for reset detection, speed handshake, token, data and handshake packet reception and transmission.
CPU Interface – The CPU interface module is clocked by CPUCLK clock and manages communication with some CPU. In this module DUSB2-ULPI core configuration and status registers are being located. CPU bus size is configurable as 8, 16 or 32-bit wide.
SRAM Interface – The SRAM interface module manages communication with Synchronous Random Access Memory. It generates address, read and write signals for the SRAM memory and buffers data bytes during the FIFO read and write operations.
EP0 endpoint –The EP0 control endpoint is special bidirectional endpoint, used for device configuration. It allows generic USB control and status access.
EP1-EP15 endpoints – The EP1 to EP15 data endpoints are unidirectional configurable double-buffered endpoints, used for application specific data transmission.

CONFIGURATION

At the synthesis level, the following parameters of the DUSB2-ULPI core can be easily adjusted to requirements of a dedicated application and technology. The CPU interface is configurable as 8, 16 or 32-bit wide. Each data endpoint can be effortlessly enabled and disabled, by simply changing an appropriate constant in the package file. There is no need to change any parts of the code, to prepare DUSB2-ULPI core with requested number of data endpoints.

– EP1_ENABLE: *TRUE (1) / FALSE (0)*
– EP2_ENABLE: *TRUE (1) / FALSE (0)*
– EP3_ENABLE: *TRUE (1) / FALSE (0)*
– EP4_ENABLE: *TRUE (1) / FALSE (0)*
– EP5_ENABLE: *TRUE (1) / FALSE (0)*
– EP6_ENABLE: *TRUE (1) / FALSE (0)*
– EP7_ENABLE: *TRUE (1) / FALSE (0)*
– EP8_ENABLE: *TRUE (1) / FALSE (0)*
– EP9_ENABLE: *TRUE (1) / FALSE (0)*
– EP10_ENABLE: *TRUE (1) / FALSE (0)*
– EP11_ENABLE: *TRUE (1) / FALSE (0)*
– EP12_ENABLE: *TRUE (1) / FALSE (0)*
– EP13_ENABLE: *TRUE (1) / FALSE (0)*
– EP14_ENABLE: *TRUE (1) / FALSE (0)*
– EP15_ENABLE: *TRUE (1) / FALSE (0)*

Besides synthesis level configuration parameters mentioned above, there is a portion of device and endpoints parameters configured at software level, after the USB bus reset condition. The following parameters can be configured at software level:

– Endpoint 0 FIFO size to 8, 16, 32 or 64 bytes
– Endpoints 1-15 FIFO size to 8, 16, 32, 64, 128, 256, 512 or 1024 bytes

– Endpoints 1-15 direction to IN or OUT
– Endpoints 1-15 mode to INTERRUPT, BULK or ISOCHRONOUS

APPLICATIONS

- Human Interface Devices e.g. keyboards, mouse and game peripherals
- Mass Storage devices like flash disk, mp3 and mp4 player
- GPS navigation system
- Digital Camera
- Cellular phone
- Audio devices like microphone and speakers
- Printer
- Scanner

PERFORMANCE

The following tables give a survey about the Core area and performance in **INTEL FPGA®** Devices after Place & Route (CPU features and peripherals included):

Device	Speed grade	cpuclk F_{max}	ulpiclk F_{max}
CYCLONE-II	-6	150 MHz	>100 MHz
CYCLONE-III	-6	180 MHz	>100 MHz
STRATIX-II	-3	250 MHz	>100 MHz
STRATIX-III	-2	270 MHz	>100 MHz
Arria GX	-6	200 MHz	>100 MHz

The area utilized by a typical configuration of the DUSB2-ULPI core suitable for HID and Mass Storage devices in vendor specific technologies, is summarized in the following table.

Component	Area	
	[LE]	[FFs]
CPU interface	270	170
ULPI interface	400	280
SRAM interface	130	95
EP0 endpoint	180	140
EP1 endpoint	190	155
EP2 endpoint	190	155
Total area	**1 360**	**995**

Core components area utilization in STRATIX-II, STRATIX-III and Arria GX families

Component	Area	
	[LE]	[FFs]
CPU interface	390	170
ULPI interface	540	280
SRAM interface	190	95
EP0 endpoint	260	140
EP1 endpoint	300	155
EP2 endpoint	300	155
Total area	**1 980**	**995**

Core components area utilization in CYCLONE-II and CYCLONE-III families

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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