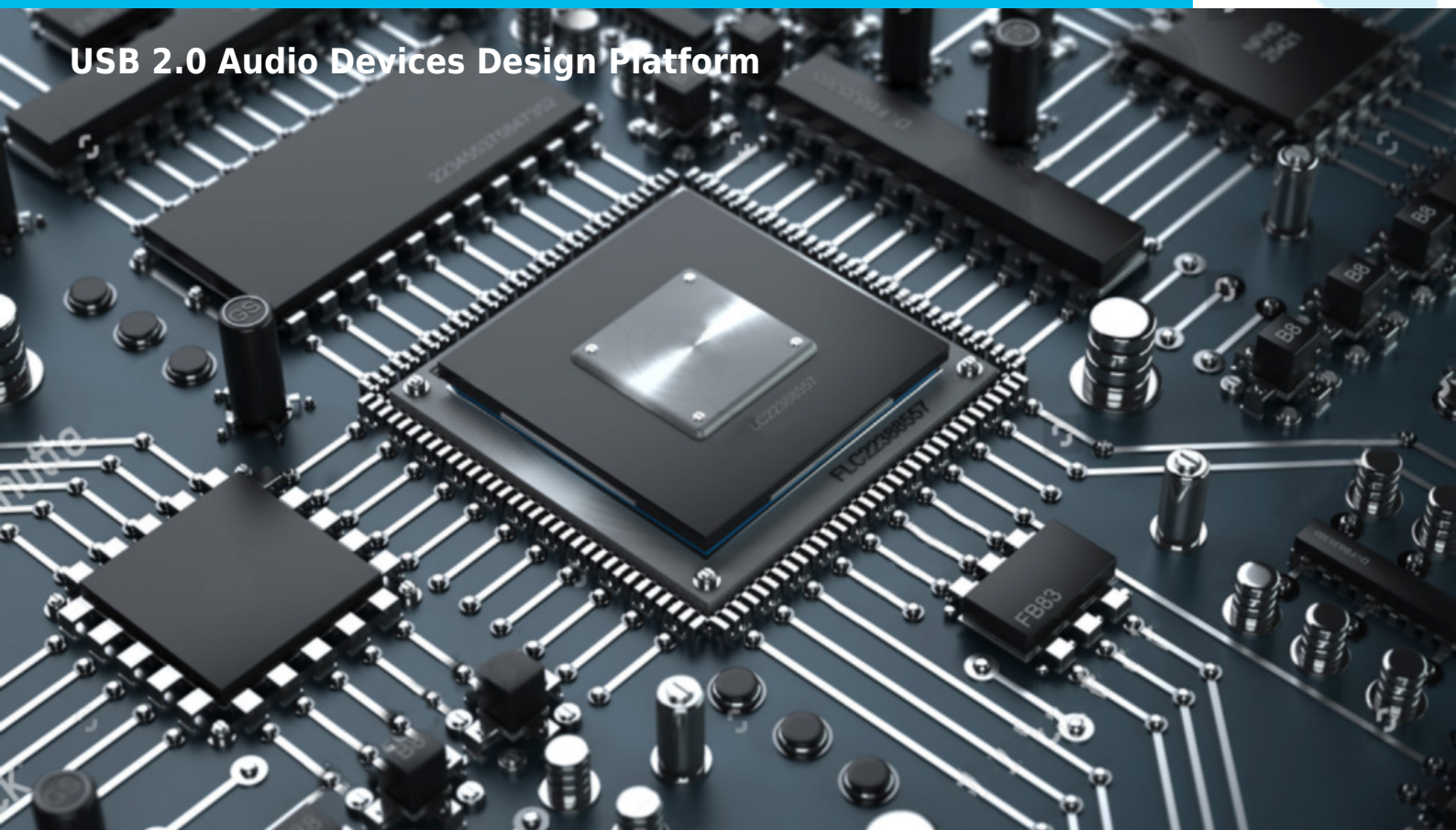
DIGITAL CORE DESIGN

AUDIO PLATFORM



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The USB 2.0 **Audio Design Platform** is a complete, integrated solution, dedicated to USB-based Audio Devices, like microphones and speakers. DCD's Audio Design Platform includes:

- DUSB2 peripheral controller designed to support 12 Mb/s "Full Speed" (FS) and 480 Mb/s "High Speed" (HS) serial data transmission rates
- DP8051XP ultra high performance, speed optimized, fully customizable 8051 8-bit microcontrollers with built-in DoCD™ debug IP core
- Audio Devices software stack optimized for DP8051XP
- FPGA board with ready-to-use, preprogrammed example USB stereo speakers application
- HAD2 – DoCD™ Hardware Assisted Debugger board
- DoCD™ Debug Software
- DoCD™ driver for Keil development software
- DoCD™ driver for IAR development software

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- Full compliance with the USB 2.0 specification
- Full-speed 12 Mbps operation
- High-speed 480 Mbps operation
- Supports UTMI Transceiver Macrocell Interface
- Synchronous RAM interface for FIFOs
- Suspend and resume power management functions
- 100% software compatible with industry standard 8051
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64K bytes of internal (on-chip) or external (off-chip) Program Memory
- Up to 16M bytes of external (off-chip) Data Memory
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- Allows operation from a wide range of CPU clock frequencies
- Fully synthesizable
- Static synchronous design
- Positive edge clocking
- No internal tri-states
- Lite design, small gate count and fast operation
- Scan test ready

UNITS SUMMARY

UTMI Interface – Clocked by the utmiclk clock, manages communication with USB 2.0 Transceiver Macrocell. It is responsible for reset detection, speed handshake, token, data and handshake packet reception and transmission.
CPU Interface – Clocked bythe cpuclk clock, manages communication with DP8051XP CPU. In this module the DUSB2 core configuration and status registers are located.
SRAM Interface – Manages communication with Synchronous Random Access Memory. Generates address, read and write signals for the SRAM memory and buffers data bytes during the FIFO read and write operations.
EP0 endpoint – A special bidirectional endpoint used for device configuration, allows generic USB control and status access.
EP1 endpoint – A unidirectional configurable endpoint used for application specific data transmission.
DP8051XP CPU – Ultra high performance, speed optimized 8-bit embedded controller, 100% software compatible with industry standard 8051.

PERFORMANCE

The following tables give a survey about the Core area and performance in **ASIC** Devices.

Device	Optimization	cpuclk F_{max}	utmiclk F_{max}
0.25u typical	area	> 200 MHz	>100 MHz
0.25u typical	speed	> 200 MHz	>100 MHz
0.18u typical	area	> 200 MHz	>100 MHz
0.18u typical	speed	> 200 MHz	>100 MHz
0.13u typical	area	> 200 MHz	>100 MHz
0.13u typical	speed	> 200 MHz	>100 MHz

The area utilized by a complete, integrated USB 2.0 HID Design Platform in vendor specific technologies, is summarized in the following table.

Component	Area [Gates]
CPU interface	1 400

UTMI interface	1 600
SRAM interface	700
EP0 endpoint	900
EP1 endpoint	1 100
DP8051XP CPU	6 300
DoCD™ debug IP core	2 200
Total area	**14 200**

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
  - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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