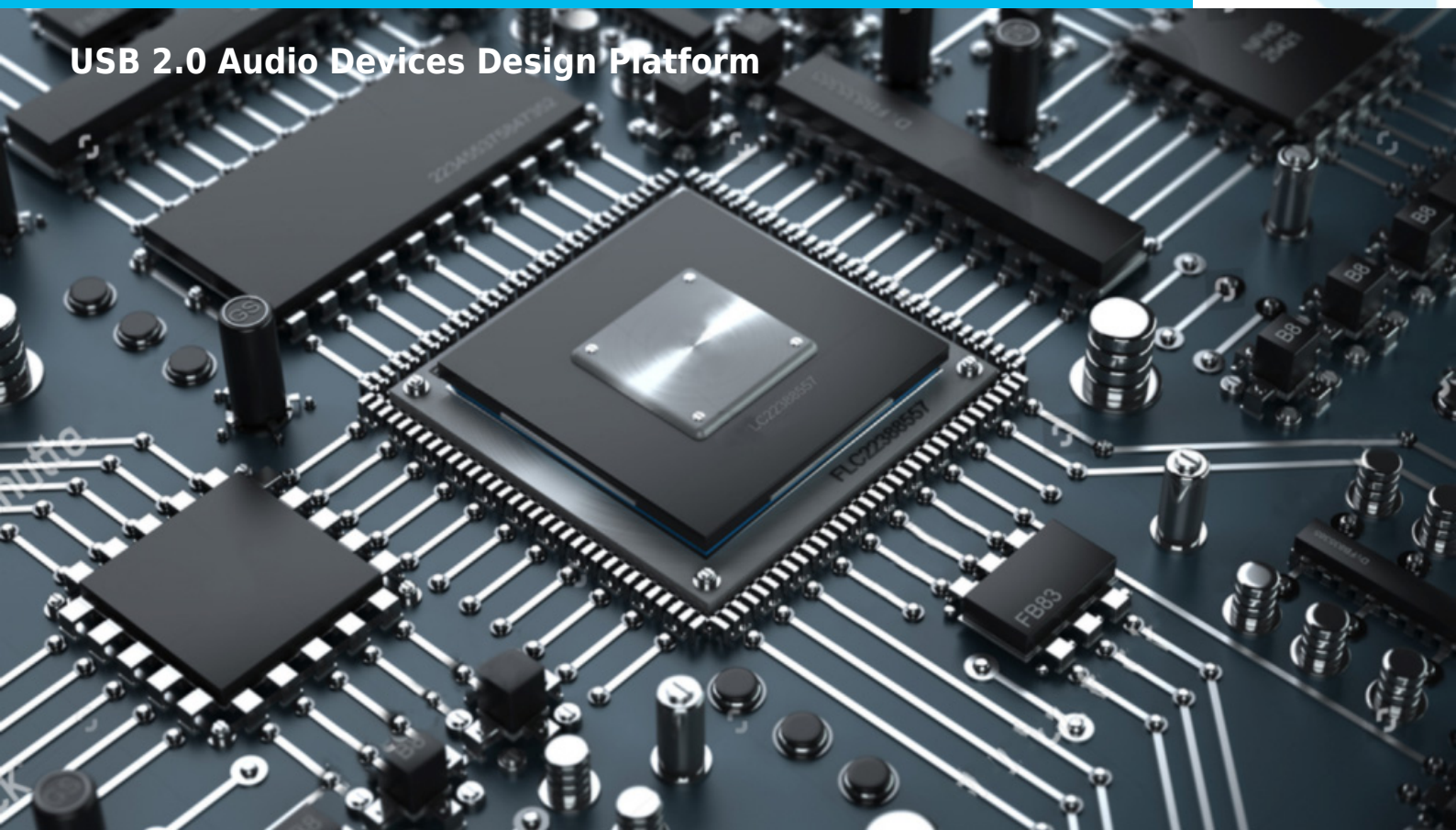
DIGITAL CORE DESIGN

AUDIO PLATFORM



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The USB 2.0 **Audio Design Platform** is a complete, integrated solution, dedicated for USB based Audio Devices, like microphone and speakers. DCD's Audio Design Platform includes:

- DUSB2 peripheral controller designed to support 12 Mb/s "Full Speed" (FS) and 480 Mb/s "High Speed" (HS) serial data transmission rates
- DP8051XP ultra high performance, speed optimized, fully customizable 8051 8-bit microcontroller with built in DoCD™ debug IP core
- Audio Devices software stack optimized for DP8051XP
- FPGA board with ready to use, preprogrammed example USB stereo speakers application
- HAD2 – DoCD™ Hardware Assisted Debugger board
- DoCD™ Debug Software
- DoCD™ driver for Keil development software
- DoCD™ driver for IAR development software

KEY FEATURES

- Full compliance with the USB 2.0 specification
- Full-speed 12 Mbps operation
- High-speed 480 Mbps operation
- Supports UTMI Transceiver Macrocell Interface
- Synchronous RAM interface for FIFOs
- Suspend and resume power management functions
- 100% software compatible with industry standard 8051
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64K bytes of internal (on-chip) or external (off-chip) Program Memory
- Up to 16M bytes of external (off-chip) Data Memory
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- Allows operation from a wide range of CPU clock frequencies
- Fully synthesizable
- Static synchronous design
- Positive edge clocking
- No internal tri-states
- Lite design, small gate count and fast operation
- Scan test ready

UNITS SUMMARY

UTMI Interface – Clocked by the utmiclk clock, manages communication with USB 2.0 Transceiver Macrocell. It is responsible for reset detection, speed handshake, token, data and handshake packet reception and transmission.
CPU Interface – Clocked bythe cpuclk clock, manages communication with DP8051XP CPU. In this module the DUSB2 core configuration and status registers are located.
SRAM Interface – Manages communication with Synchronous Random Access Memory. Generates address, read and write signals for the SRAM memory and buffers data bytes during the FIFO read and write operations.
EP0 endpoint – A special bidirectional endpoint used for device configuration, allows generic USB control and status access.
EP1 endpoint – A unidirectional configurable endpoint used for application specific data transmission.
DP8051XP CPU – Ultra high performance, speed optimized 8-bit embedded controller, 100% software compatible with industry standard 8051.

PERFORMANCE

The following tables give a survey about the Core area and performance in Programmable Logic Devices after Place & Route (including CPU features and peripherals):

Device	Speed grade	cpuclk F_{max}	utmiclk F_{max}
CYCLONE-II	-6	60 MHz	>100 MHz
CYCLONE-III	-6	70 MHz	>100 MHz
STRATIX-II	-3	100 MHz	>100 MHz
STRATIX-III	-2	110 MHz	>100 MHz
ARRIA GX	-6	80 MHz	>100 MHz

Core performance in Intel FPGA® devices

The area utilized by a complete, integrated USB 2.0 HID Design Platform in vendor specific technologies, is summarized in the following table.

Component	Area	
	[LE]	[FFs]
CPU interface	270	170
UTMI interface	310	230
SRAM interface	130	95
EP0 endpoint	180	140
EP1 endpoint	190	155
DP8051XP CPU	1 220	320
DoCD™ debug IP core	450	270
Total area	**2 750**	**1 380**

Core components area utilization in STRATIX-II, STRATIX-III and Arria GX families

Component	Area	
	[LE]	[FFs]
CPU interface	390	170
UTMI interface	450	230
SRAM interface	190	95

EP0 endpoint	260	140
EP1 endpoint	300	155
DP8051XP CPU	1 850	320
DoCD™ debug IP core	600	270
Total area	**4 040**	**1 380**

Core components area utilization in CYCLONE-II and CYCLONE-III families

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 3 months maintenance
  - Delivery of the IP Core and documentation updates, minor and major versions changes
  - Phone & email support

LICENSING

Transparent and clearly defined licensing methods without royalty-per-chip fees, make use of our IP Cores easy & simple.
– ***Single-Site license option*** – dedicated to small and middle sized companies, which run their business in one place.
– ***Multi-Site license option*** – dedicated to corporate customers who operate at several locations. The licensed product can be used in selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.
There are two formats of the delivered IP Core:
– VHDL or Verilog RTL synthesizable HDL Source code
– FPGA EDIF/NGO/NGD/QXP/VQM Netlist

CONTACT

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