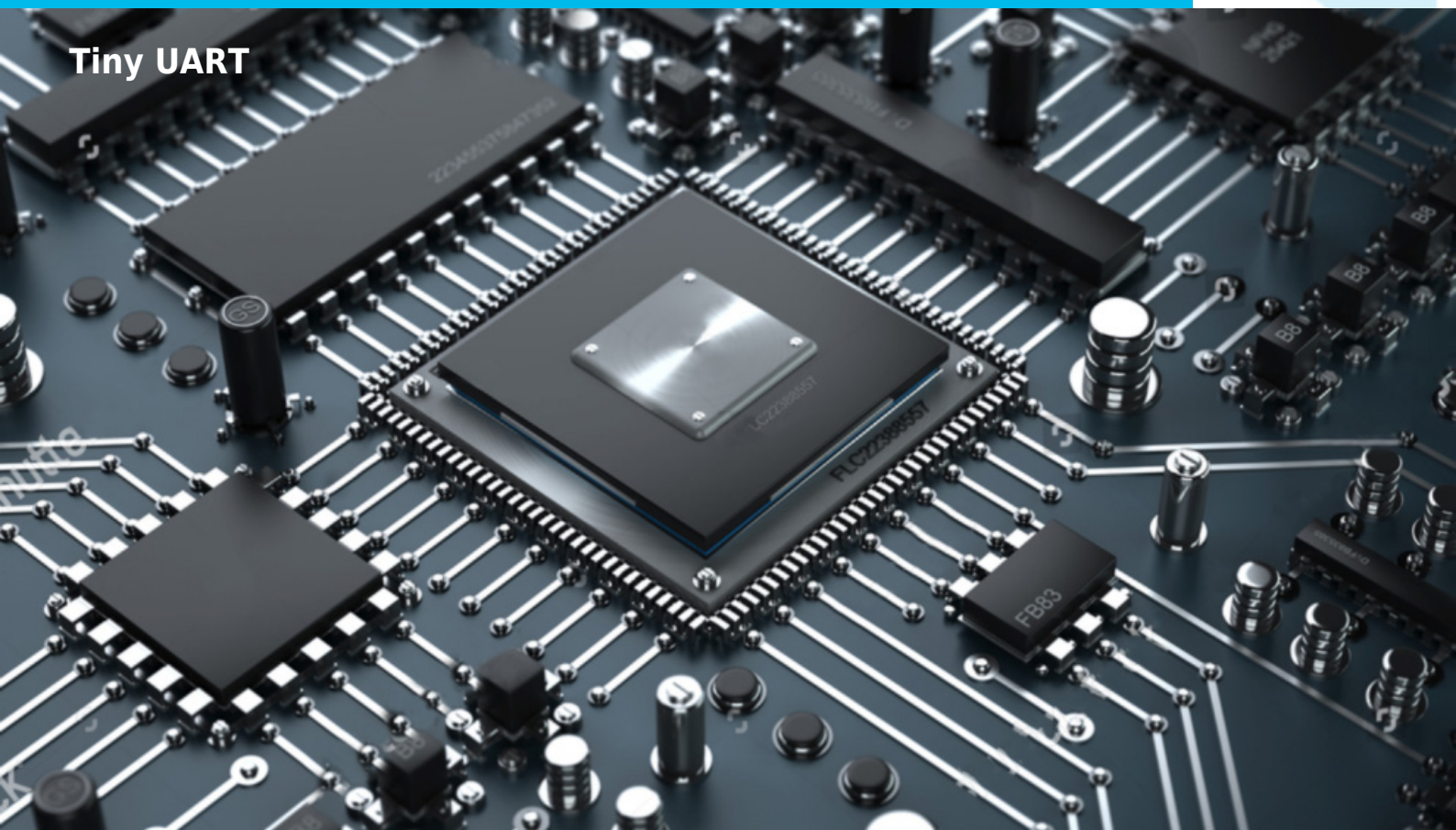
DIGITAL CORE DESIGN

DUART



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DµART bridge to APB, AHB, AXI bus, it is a soft core of a Universal Asynchronous Receiver/Transmitter (UART). It performs **serial-to-parallel** conversion on data characters received from a peripheral device or MODEM, and **parallel-to-serial** conversion on data characters received from the CPU. The CPU can read a complete status of the UART at any time during the functional operation. The reported status information includes a type and condition of the transfer operations performed by the UART, as well as any error conditions (overrun, framing). The DµART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1), and producing 16 × clock for driving internal transmitter logic. Provisions are also included to use this 16 × clock to drive the receiver logic. **The DµART has a processor-interrupt system**. Interrupts can be programmed in accordance to your requirements, minimizing computing required to handle the communication link. The core is perfect for applications where the UART Core and microcontroller are clocked by the same clock signal and are implemented inside the same ASIC or FPGA chip, as well as for standalone implementation, where several UARTs are required to be implemented inside a single chip, and driven by some off-chip devices.

Watch the DµART presentation on DCD's You Tube:

KEY FEATURES

- Majority Voting Logic
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data
- In UART mode receiver and transmitter are double buffered to eliminate the need for precise synchronization between the CPU and serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- 16 bit programmable baud generator
- False start bit detection
- Line break generation and detection. Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Overrun, framing error detection
- Full prioritized interrupt system controls
- Technology independent HDL Source Code
- Fully synthesizable static design with no internal tri-state buffers
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

UNITS SUMMARY

RST – Global Reset. When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The states of various output signals (SO, INTR, OUT 1, OUT 2, RTS, DTR) are affected by an active RST input.
DATAI(7:0), DATAO(7:0) – Data Busses, the bus provides communications between the UART and CPU. Data, control words, and status information are transferred via the Data Bus.
ADDR(2:0), Address Bus – selects a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown in figure below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.
RD – Read. When RD is low and chip is selected, the CPU can read status information or data from selected UART register.
WR – Write, When WR is low while the chip is selected, the CPU can write control words or data into selected UART register.
CS – Chip Select, When CS is low, the chip is selected. This enables communication between the UART and CPU.
RXD – Serial Input. Serial data input from the communications link (peripheral device, MODEM, or data set).
INTR – Interrupt pin goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available: timeout (FIFO Mode only); Transmitter Holding Register Empty; and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.
TEMT – Transmitter Empty. This pin can be used in RS485 systems to control three state output buffer. When in low state, the output buffer should be enabled, to allow transmission from DUART. High state on TEMT informs that transmitter in IDLE state, or reception is in progress (in Half Duplex mode, transmission is disabled as long as the reception is in progress).
TXD – Serial Output. Composite serial data output to the communications link (peripheral, MODEM or data set). The TXD signal is set to the logic 1 state upon a Master Reset operation.

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	Speed grade	LE/ALM	MEMORY Bits	F_{max}
ARIA GX	-6	143/130	–	267 MHz
ARIA V	-6	100/141	–	315 MHz
CYCLONE	-6	218	–	226 MHz
CYCLONE2	-6	218	–	297 MHz
CYCLONE3	-6	227	–	335 MHz
CYCLONE4	-6	223	–	317 MHz
CYCLONE5	-6	102/141	–	265 MHz
STRATIX	-5	218	–	244 MHz
STRATIX2	-3	144/131	–	404 MHz
STRATIX3	-2	146/130	–	542 MHz
STRATIX4	-2	146/130	–	605 MHz
STRATIX5	-2	95/148	–	637 MHz
STRATIX GX	-5	218	–	242 MHz
STRATIX2 GX	-3	218	–	176 MHz
MAX II	– 4	218		91 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

Digital Core Design Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: 0048 32 282 82 66
fax: 0048 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/