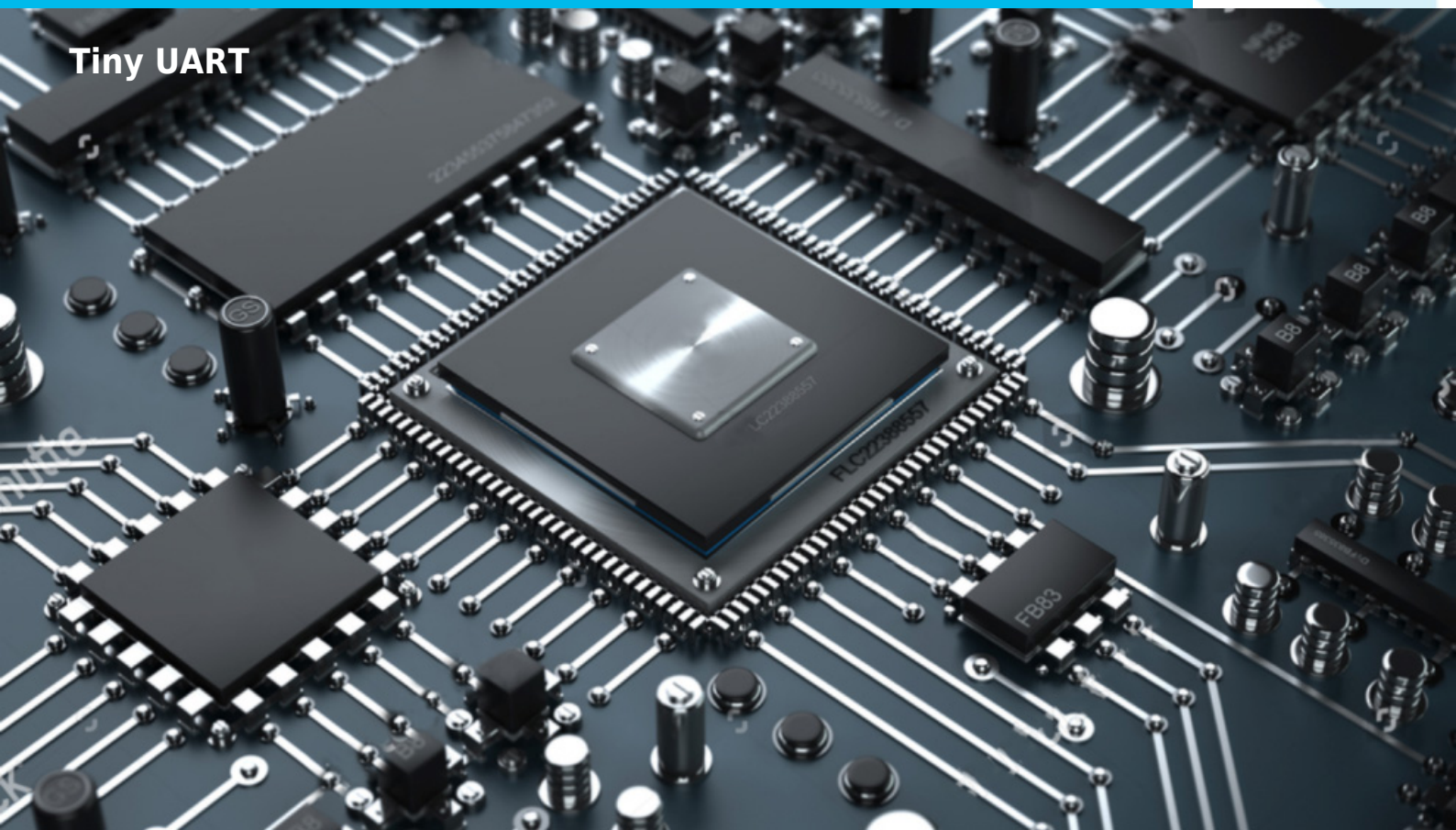
DIGITAL CORE DESIGN

DUART



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DµART UART IP Core – High-Performance Soft UART for FPGA & ASIC

The **DµART** from **DCD-SEMI** is a **soft core Universal Asynchronous Receiver/Transmitter (UART)**, designed for seamless integration into **APB, AHB, and AXI bus architectures**. It provides **high-efficiency serial communication** while minimizing CPU load, making it ideal for both **embedded systems and standalone UART implementations**.

Efficient Serial-to-Parallel Data Conversion

The DµART performs:

- **Serial-to-parallel conversion** on data received from peripheral devices or MODEMs
- **Parallel-to-serial conversion** for data transmitted from the CPU
- Provides complete status information to the CPU, including transfer type, operation status, and **error conditions such as overrun and framing**

This ensures **reliable and predictable UART communication** in complex SoC and FPGA designs.

Programmable Baud Rate Generator

The core includes a **flexible baud rate generator**:

- Divides timing reference clock input by divisors of **1 to (2^{16}–1)**
- Produces **16× clocks** to drive transmitter logic
- Can also drive receiver logic, supporting **high-precision UART timing**

This flexibility allows the DµART to work in **synchronous systems with CPU clock alignment** or in **standalone multi-UART environments**.

Advanced Interrupt System

- **Processor-interrupt system** configurable to application requirements
- Reduces CPU overhead for **data handling and serial communication management**
- Supports **polling or interrupt-driven operation**, ideal for low-power or high-throughput designs

Key Features

- Soft core UART compatible with **ASIC and FPGA designs**
- Full support for **internal CPU interfacing** via APB, AHB, or AXI
- High-performance **serial communication with minimal CPU load**
- Configurable **baud rates and clocking**
- Error detection for **overrun and framing errors**
- Scalable for **standalone or multi-UART systems**

Ideal Applications

- Embedded systems requiring **reliable UART communication**
- FPGA or ASIC implementations with multiple UART channels
- Industrial automation, telecom, and IoT applications
- Legacy system replacements where **soft UART cores** are needed

Verification-Ready and Technology Independent

Like all DCD-SEMI UART cores, **DµART** comes with:

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- A **fully automated testbench**
- Complete **validation suite** for easy SoC integration
- Technology-independent design for **implementation across multiple FPGA and ASIC processes**

UART IP Core Family Comparison

The table below compares DCD-SEMI UART and serial communication IP Cores to help FPGA and ASIC design engineers quickly select the optimal solution for their project requirements.

Feature / IP Core	D16450	D16550	D16750	D16752	D16950	D8530	DMESCC	D26C92	DµART
Primary Function	Classic UART	FIFO-based UART	High-performance UART	Dual-channel high-performance UART	High-throughput UART	Dual-channel USART	Dual-channel multiprotocol serial controller	Dual-channel UART / DUART	Lightweight soft UART
UART Compatibility	16450 / TL16C450	16550 / TL16C550A	16750 / TL16C750	16752 / TL16C752	16450-16750 + OX16C950	Zilog 8530-compatible	Enhanced ESCC-compatible	SC26C92 / SCC2692 / SCN2681 compatible	Generic UART / custom soft core
Channels	1	1	1	2	1	2	2	2	1
Supported Modes	Asynchronous	Asynchronous & FIFO	Asynchronous & FIFO	Asynchronous & FIFO, dual-channel	Asynchronous & synchronous	Asynchronous & synchronous	Asynchronous & synchronous	Asynchronous & FIFO, dual-channel	Asynchronous
FIFO Support	▯ No FIFO	▯ 16-byte FIFO	▯ 512-byte FIFO	▯ 64-byte FIFO per channel	▯ 128-byte FIFO	Optional / limited	Optional / configurable	▯ 8-character RX/TX FIFO per channel	▯ No FIFO
FIFO Trigger Levels	—	Configurable	Programmable (1-512)	Programmable per channel	Programmable (1-127)	—	—	Programmable per channel	—
CPU Load	High	Medium	Low	Low	Low	Medium	Medium	Medium	Low
Error Reporting	Parity, framing, overrun, break	Parity, framing, overrun, break	Parity, framing, overrun, break	Parity, framing, overrun, break, idle	Parity, framing, overrun, break	Parity, CRC, abort	Parity, CRC, abort	Parity, framing, overrun, break	Overrun, framing
CRC Generation / Check	No	No	No	No	No	Yes (sync modes)	Yes (sync modes)	No	No
Modem Control	Full	Full	Advanced autoflow	Hardware/software flow control, TCR	Advanced autoflow	Yes (both channels)	Yes (both channels)	Yes, DMA & modem interface	Optional via software
Interrupt System	Programmable	Programmable	Advanced programmable	Programmable, FIFO RDY register	Advanced programmable	Programmable	Programmable	Programmable, independent per channel	Lightweight programmable
DMA Support	Interrupt-optimized	Interrupt-optimized	Yes	Yes	Yes	Yes	Yes	Yes	Optional
Clocking Options	Internal BRG	Internal BRG	Internal / external	Internal / external	Internal / external	Internal BRG	Internal BRG	Independent programmable clock, external or 16× derived	Internal / external programmable
Special Features	Legacy compatibility	Configurable FIFO & Modem	Deep FIFO (512B), autoflow, 16450 modes	Dual-channel, FIFO RDY register, hardware/software flow control, TCR	Deep FIFO, 9-bit mode, synchronous	Legacy protocol support (HDLC, SDLC)	Enhanced block transfer, vectored interrupts	Independent channel baud rates, watchdog timers, dual-speed operation	Lightweight, flexible baud rate, minimal CPU load, standalone or integrated use
Typical Applications	Legacy UART replacement	FIFO-based legacy upgrade	High-throughput UART, legacy replacement	Dual-channel embedded UART, TL16C752 replacement	Telecom, industrial gateways	Telecom, LAN, industrial serial	Communications controllers, protocol engines	Dual-speed terminals, embedded dual UART systems, SC26C92 replacement	Embedded soft UART, low-resource FPGA/ASIC designs
Bus Interfaces	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI
Technology Independence	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Selection Guidelines

- **D16450:** Exact legacy 16450 / TL16C450 replacement.
- **D16550:** FIFO buffering and moderate CPU optimization.
- **D16750:** High-performance UART with deep FIFO and low CPU load.
- **D16752:** Dual-channel UART with 64-byte FIFOs, hardware/software flow control, TCR.
- **D16950:** High-throughput UART with deep FIFO, synchronous mode, and advanced flow control.
- **D8530:** Dual-channel USART for legacy protocol support.
- **DMESCC:** Advanced multiprotocol serial communication and block handling.
- **D26C92:** Dual-channel SC26C92 / SCC2692 / SCN2681 replacement with watchdog timers.
- **DµART:** Lightweight soft UART, minimal CPU load, flexible baud rate, ideal for embedded FPGA/ASIC systems.

Watch the DµART presentation on DCD's You Tube:

As Seen On YouTube

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Majority Voting Logic
- Adds or deletes standard asynchronous communication bits (start, stop, and parity) to or from serial data
- In UART mode receiver and transmitter are double buffered to eliminate the need for precise synchronization between the CPU and serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- 16 bit programmable baud generator
- False start bit detection
- Line break generation and detection. Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Overrun, framing error detection
- Full prioritized interrupt system controls
- Technology independent HDL Source Code
- Fully synthesizable static design with no internal tri-state buffers

UNITS SUMMARY

RST – Global Reset. When this input is high, it clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the UART. The states of various output signals (SO, INTR, OUT 1, OUT 2, RTS, DTR) are affected by an active RST input.
DATAI(7:0), DATAO(7:0) – Data Busses, the bus provides communications between the UART and CPU. Data, control words, and status information are transferred via the Data Bus.
ADDR(2:0), Address Bus – selects a UART register for the CPU to read from or write to during data transfer. A table of registers and their addresses is shown in figure below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.
RD – Read. When RD is low and chip is selected, the CPU can read status information or data from selected UART register.
WR – Write, When WR is low while the chip is selected, the CPU can write control words or data into selected UART register.
CS – Chip Select, When CS is low, the chip is selected. This enables communication between the UART and CPU.
RXD – Serial Input. Serial data input from the communications link (peripheral device, MODEM, or data set).
INTR – Interrupt pin goes high whenever any one of the

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following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available: timeout (FIFO Mode only); Transmitter Holding Register Empty; and MODEM Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset operation.

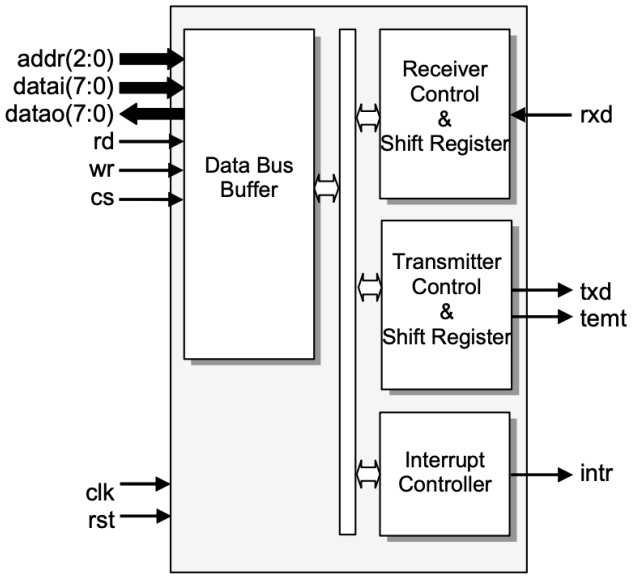
TEMT – Transmitter Empty. This pin can be used in RS485 systems to control three state output buffer. When in low state, the output buffer should be enabled, to allow transmission from DUART. High state on TEMT informs that transmitter in IDLE state, or reception is in progress (in Half Duplex mode, transmission is disabled as long as the reception is in progress).

TXD – Serial Output. Composite serial data output to the communications link (peripheral, MODEM or data set). The TXD signal is set to the logic 1 state upon a Master Reset operation.

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

BLOCK DIAGRAM



PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA** devices after Place & Route:

Device	Speed grade	LE/ALM	MEMORY Bits	F_{max}
ARIA GX	-6	143/130	–	267 MHz
ARIA V	-6	100/141	–	315 MHz
CYCLONE	-6	218	–	226 MHz
CYCLONE2	-6	218	–	297 MHz
CYCLONE3	-6	227	–	335 MHz
CYCLONE4	-6	223	–	317 MHz
CYCLONE5	-6	102/141	–	265 MHz
STRATIX	-5	218	–	244 MHz
STRATIX2	-3	144/131	–	404 MHz
STRATIX3	-2	146/130	–	542 MHz
STRATIX4	-2	146/130	–	605 MHz
STRATIX5	-2	95/148	–	637 MHz
STRATIX GX	-5	218	–	242 MHz
STRATIX2 GX	-3	218	–	176 MHz
MAX II	– 4	218		91 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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