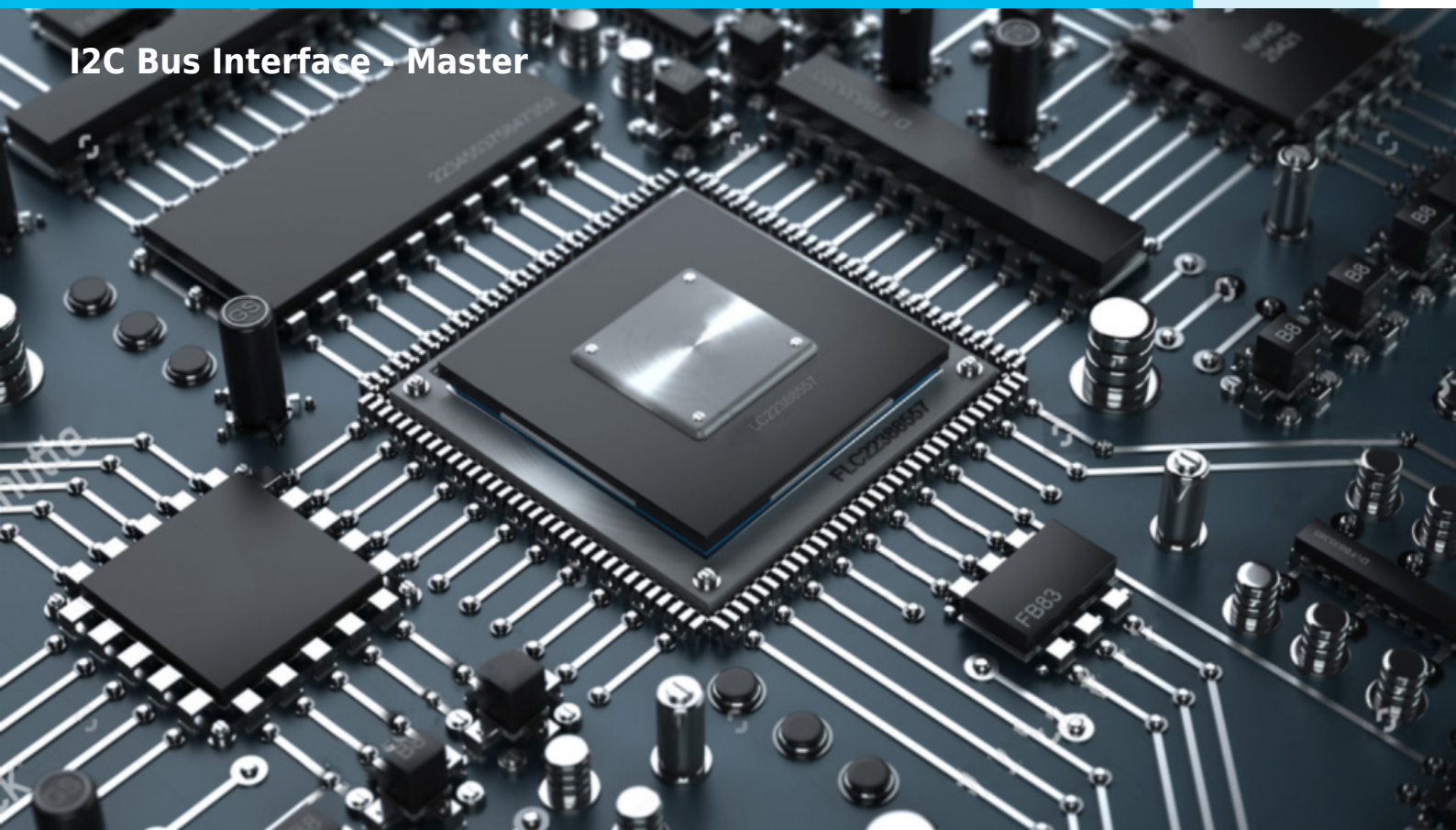
DIGITAL CORE DESIGN

DI2CM

I2C Bus Interface - Master



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DI2CM IP Core – I2C Master Controller for FPGA & ASIC

The **DI2CM IP Core** from **DCD-SEMI** is a robust and configurable **I2C master controller** designed to provide a seamless interface between a **microprocessor or microcontroller** and an **I2C bus** in modern **FPGA and ASIC designs**. Delivered as a flexible **bridge to APB, AHB, and AXI bus architectures**, DI2CM enables reliable I2C communication in embedded, industrial, and system-control applications.

The core operates exclusively in **master mode**, functioning as either a **master transmitter** or a **master receiver**, with the operating mode fully controlled by software running on the host processor.

Full Compliance with the Latest I2C Specification

DI2CM incorporates all essential features defined in the **latest I2C specification**, ensuring compatibility with a wide range of I2C-compliant peripherals and systems. Supported features include:

- **Multi-master arbitration**
- **Clock synchronization**
- **High-speed transmission mode**
- Reliable operation in complex **multi-master environments**

These capabilities make DI2CM suitable for both simple point-to-point designs and advanced multi-device I2C systems.

Flexible Timing and Clock Support

A built-in **programmable timer** allows the DI2CM IP Core to operate across a **wide range of system clock frequencies**, simplifying integration into diverse SoC architectures without the need for external clocking logic. This flexibility ensures stable I2C timing across different FPGA families and ASIC process technologies.

SoC-Friendly Integration

The DI2CM IP Core is a **technology-independent design** that can be implemented in a variety of **FPGA and ASIC processes**. To support modern SoC architectures, the core can be delivered with the following host interfaces:

- **AMBA APB**
- **AMBA AHB**
- **AMBA AXI**

This scalability allows DI2CM to fit seamlessly into both **deeply embedded systems** and **high-performance SoC platforms**.

Typical Applications

- Embedded microcontroller-based systems
- System configuration and control
- Sensor and peripheral management
- Industrial and consumer electronics
- FPGA-based SoCs requiring I2C master functionality

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.co .

KEY FEATURES

- Conforms to v.3.0 of the I2C specification
- Master operation
  - Master transmitter
  - Master receiver
- Support for all transmission speeds
  - Standard (up to 100 kb/s)
  - Fast (up to 400 kb/s)
  - Fast Plus (up to 1 Mb/s)
  - High Speed (up to 3,4 Mb/s)
- Arbitration and clock synchronization
- Support for multi-master systems
- Support for both 7-bit and 10-bit addressing formats on the I2C bus

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- Interrupt generation
- Build-in 8-bit timer for data transfers speed adjusting
- Host side interface dedicated for microprocessors/microcontrollers
- User-defined timing (data setup, start setup, start hold, etc.)
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

UNITS SUMMARY

CPU Interface – Performs the interface functions between DI2CM internal blocks and microprocessor. Allows easy connection between the core and a microprocessor / microcontroller system.
Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.
Shift Register – Controls SDA line, performs data and address shifts, during the data transmission and reception.
Control Register – Contains five control bits, used for performing all types of I^2C Bus transmissions.
Status Register – Contains seven status bits that indicate state of the I^2C Bus and the DI2CM core.
Clock Generator – Performs generation of the serial clock.
Input Filter – Performs spike filtering.
Clock Synchronization – Performs clock synchronization.
Arbitration Logic – Performs arbitration during operations in multi-master systems.
Timer – Allows operation from a wide range of the input frequencies. It is programmed by the user before transmission and can be reprogrammed to change the SCL frequency.

PERFORMANCE

The following table gives a survey about the Core area and performance in **LATTICE FPGA** devices after Place & Route (all key features included):

Device	Speed grade	LUTs/PFUs	F_{max}
SC	-7	295 / 124	301 MHz
ECP2	-7	285 / 120	253 MHz
ECP2M	-7	239 / 120	253 MHz
XP2	-7	239 / 120	210 MHz
EC	-5	340 / 120	185 MHz
ECP	-5	340 / 120	183 MHz
XP	-5	340 / 120	155 MHz
ispXPGA	-5	363 / 103	107 MHz
ORCA 4	-3	387 / 57	69 MHz
ORCA 3	-7	316 / 57	43 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Remote Access license option* – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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