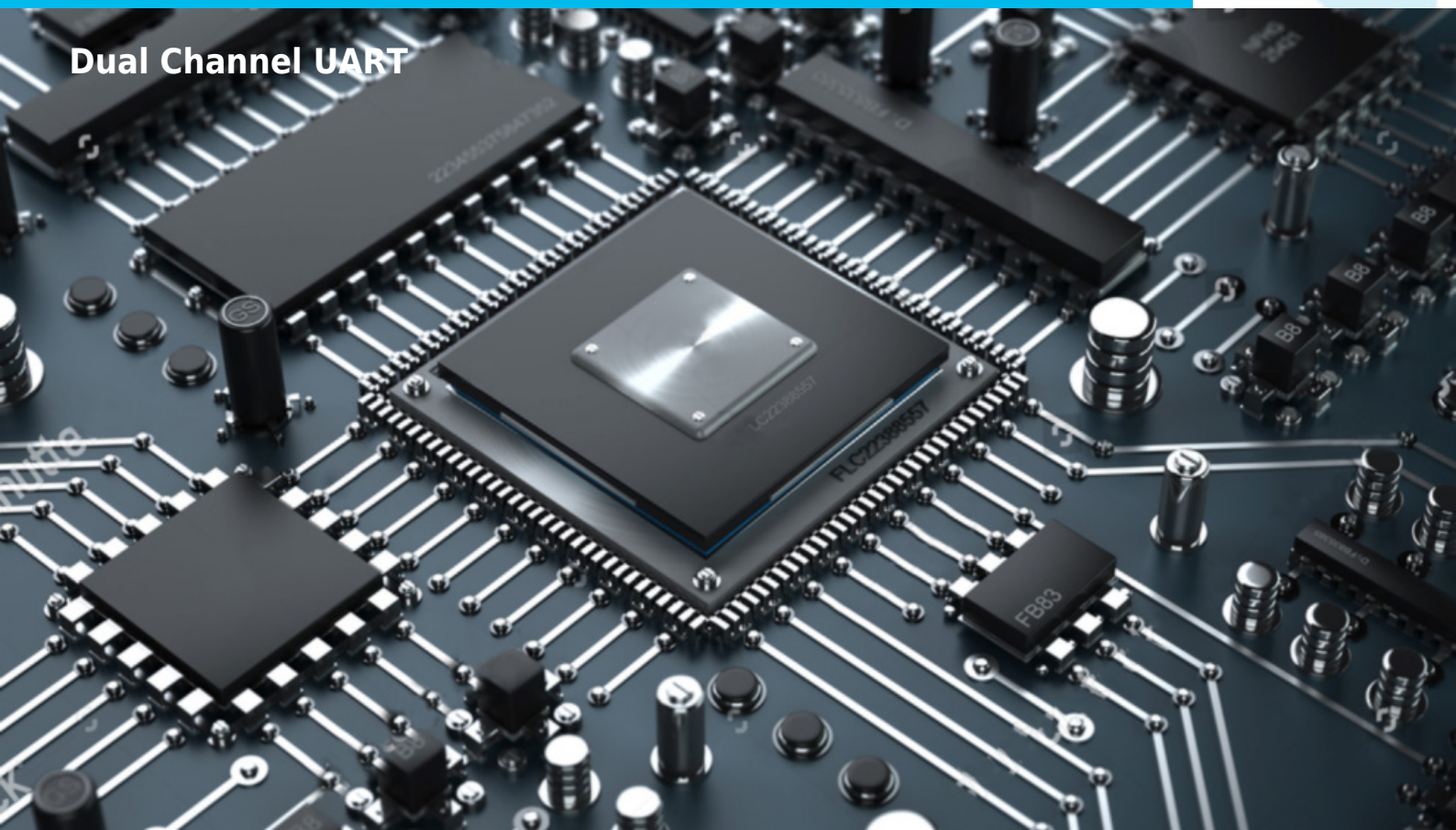
DIGITAL CORE DESIGN

D2692

Dual Channel UART



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D26C92 Dual UART IP Core – SC26C92 / SCC2692 / SCN2681 Compatible

The **D26C92 UART IP Core** from **DCD-SEMI** is a **high-performance dual-channel Universal Asynchronous Receiver/Transmitter (DUART)** designed for **FPGA and ASIC integration**. Delivered as a **bridge to APB, AHB, and AXI bus architectures**, it is **software compatible with SC26C92, SCC2692, and SCN2681**, offering additional features and **enhanced FIFOs** for demanding serial communication applications.

Dual-Channel Full-Duplex Communication

The D26C92 provides **two independent full-duplex UART channels** in a single core:

- Each channel includes **8-character receive and transmit FIFOs**
- **Mode register 0** and **extended baud rate** support
- Independent **receiver and transmitter configuration** for flexible multi-speed operation
- Optional **DMA and modem interface** support

This makes the D26C92 ideal for **dual-speed channel applications**, such as **clustered terminal systems** or **multi-protocol communication interfaces**.

Programmable Baud Rate and Timing Control

Each channel can select its operating speed from **27 fixed baud rates**, a **16× clock derived from a programmable counter/timer**, or an **external 1× or 16× clock**.

- **Baud rate generator** supports both crystal and external clock inputs
- Independent speed configuration allows simultaneous operation at **different baud rates per channel**

This flexibility makes it highly suitable for **complex multi-device serial networks**.

Advanced Interrupt and Watchdog Support

The D26C92 core includes:

- **Programmable receiver and transmitter interrupts** for efficient CPU offload
- **Watchdog timer** for each receiver to ensure data integrity
- Polled or interrupt-driven operation to fit a variety of **embedded system architectures**

FIFO-Enhanced Architecture

The built-in FIFOs improve system performance by **reducing CPU intervention** during high-speed data transmission:

- **8-character depth for both RX and TX FIFOs**
- Handles high-throughput communication with **low CPU load**
- Supports **dual-speed channel operation** for multi-device systems

Flexible and Configurable Interfaces

The D26C92 core is **fully configurable** to meet project-specific requirements:

- Each channel can operate independently with different **baud rates and data formats**
- Supports **full-duplex operation**, **modem interface**, and **DMA transfers**
- Compatible with standard **APB, AHB, and AXI interfaces**

Ideal Applications

- Dual-speed terminal clusters and legacy system upgrades

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- Industrial automation and control systems
- Multi-protocol communication devices
- FPGA and ASIC SoC designs requiring **dual UART channels**
- Systems requiring software-compatible SC26C92 / SCC2692 / SCN2681 replacement

Verification-Ready and Technology Independent

Like all DCD-SEMI UART IP Cores, the **D26C92** includes a **fully automated testbench** and **complete validation suite**, enabling **quick integration into SoC and FPGA designs**.

- Technology-independent design suitable for a wide range of **FPGA and ASIC process nodes**
- Optimized for **low logic utilization and high throughput**

UART IP Core Family Comparison

The table below compares DCD-SEMI UART and serial communication IP Cores to help FPGA and ASIC design engineers quickly select the optimal solution for their project requirements.

Feature / IP Core	D16450	D16550	D16750	D16752	D16950	D8530	DMESCC	D26C92
Primary Function	Classic UART	FIFO-based UART	High-performance UART	Dual-channel high-performance UART	High-throughput UART	Dual-channel USART	Dual-channel multiprotocol serial controller	Dual-channel UART / DUART
UART Compatibility	16450 / TL16C450	16550 / TL16C550A	16750 / TL16C750	16752 / TL16C752	16450-16750 + OX16C950	Zilog 8530-compatible	Enhanced ESCC-compatible	SC26C92 / SCC2692 / SCN2681 compatible
Channels	1	1	1	2	1	2	2	2
Supported Modes	Asynchronous	Asynchronous & FIFO	Asynchronous & FIFO	Asynchronous & FIFO, dual-channel	Asynchronous & synchronous	Asynchronous & synchronous	Asynchronous & synchronous	Asynchronous & FIFO, dual-channel
FIFO Support	▯ No FIFO	▯ 16-byte FIFO	▯ 512-byte FIFO	▯ 64-byte FIFO per channel	▯ 128-byte FIFO	Optional / limited	Optional / configurable	▯ 8-character RX/TX FIFO per channel
FIFO Trigger Levels	—	Configurable	Programmable (1–512)	Programmable per channel	Programmable (1–127)	—	—	Programmable per channel
CPU Load	High	Medium	Low	Low	Low	Medium	Medium	Medium
Error Reporting	Parity, framing, overrun, break	Parity, framing, overrun, break	Parity, framing, overrun, break	Parity, framing, overrun, break, idle	Parity, framing, overrun, break	Parity, CRC, abort	Parity, CRC, abort	Parity, framing, overrun, break
CRC Generation / Check	No	No	No	No	No	Yes (sync modes)	Yes (sync modes)	No
Modem Control	Full	Full	Advanced autoflow	Hardware/software flow control, TCR	Advanced autoflow	Yes (both channels)	Yes (both channels)	Yes, DMA & modem interface
Interrupt System	Programmable	Programmable	Advanced programmable	Programmable, FIFO RDY register	Advanced programmable	Programmable	Programmable	Programmable, independent per channel
DMA Support	Interrupt-optimized	Interrupt-optimized	Yes	Yes	Yes	Yes	Yes	Yes
Clocking Options	Internal BRG	Internal BRG	Internal / external	Internal / external	Internal / external	Internal BRG	Internal BRG	Independent programmable clock, external or 16× derived
Special Features	Legacy compatibility	Configurable FIFO & Modem	Deep FIFO (512B), autoflow, 16450 modes	Dual-channel, FIFO RDY register, hardware/software flow control, TCR	Deep FIFO, 9-bit mode, synchronous	Legacy protocol support (HDLC, SDLC)	Enhanced block transfer, vectored interrupts	Independent channel baud rates, watchdog timers, dual-speed operation
Typical Applications	Legacy UART replacement	FIFO-based legacy upgrade	High-throughput UART, legacy replacement	Dual-channel embedded UART, TL16C752 replacement	Telecom, industrial gateways	Telecom, LAN, industrial serial	Communications controllers, protocol engines	Dual-speed terminals, embedded dual UART systems, SC26C92 replacement
Bus Interfaces	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI
Technology Independence	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Selection Guidelines

- **Choose D16450** for exact legacy 16450 / TL16C450 replacement.
- **Choose D16550** when FIFO buffering and moderate CPU optimization are required.
- **Choose D16750** for high-performance legacy replacement with deep FIFO and low CPU load.
- **Choose D16752** for **dual-channel high-performance UART** with hardware/software flow control and 64-byte FIFOs.
- **Choose D16950** for high-throughput UART with deep FIFO, synchronous mode, and advanced flow control.
- **Choose D8530** when dual-channel USART and legacy protocol support are required.
- **Choose DMESCC** for advanced multiprotocol serial communication and block handling.
- **Choose D26C92** for **dual-channel SC26C92 / SCC2692 / SCN2681 replacement** with independent baud rates, watchdog timers, and FIFO support.

Watch the D2692 presentation on DCD's YouTube:

As Seen On YouTube

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Software compatible with SC26C92, SCC2692 and SCN2681 UARTs
- Configuration capability
- Dual full-duplex independent asynchronous receiver/transmitters
- 8 character FIFOs for each receiver and transmitter
- Programmable data format:
  - 5 to 8 data bits plus parity
  - Odd, even, no parity or force parity
  - 1, 1.5 or 2 stop bits programmable in 1/16-bit increments
- 16-bit programmable Counter/Timer
- Programmable baud rate for each receiver and transmitter selectable from:
  - 27 fixed rate
  - Other baud rates – at 16X
  - Programmable user-defined rates derived from a programmable counter/timer
  - External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode:

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- Normal (full-duplex)
- Automatic echo
- Local loopback
- Remote loopback
- Multidrop mode (also called ‘wake-up’ or ‘9-bit’)

- Multi-function 7-bit input port:
  - Can serve as clock, modem, or control inputs
  - Change of state detection on four inputs
- Multi-function 8-bit output port:
  - Individual bit set/reset capability
  - Outputs can be programmed to be status/interrupt signals
  - FIFO states for DMA and modem interface
- Versatile interrupt system:
  - Single interrupt output with eight maskable interrupting conditions
  - Output port can be configured to provide a total of up to six separate wire-ORable interrupt outputs
  - Each FIFO can be programmed for four different interrupt levels
  - Watch dog timer for each receiver
- Automatic wake-up mode for multidrop applications
- Start-end break interrupt/status
- Detects break which originates in the middle of a character
- Power down mode
- Receiver timeout mode

UNITS SUMMARY

Data Bus Buffer – Provides an interface between external and internal data buses. It is controlled by the operation control block allowing read and write operations to take place between the controlling CPU and the DUART. **Operation Control** – Receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus. **Interrupt Control** – A single active-Low interrupt output (INTR) is provided which is activated upon occurrence of any of eight internal events. Associated with the interrupt system are the Interrupt Mask Register (IMR) and the Interrupt Status Register (ISR). The IMR can be programmed to select only certain conditions to cause INTR to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions. Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitter, receivers, and counter/timer. When OP3 to OP7 are programmed as interrupts, their output buffers are changed to the open drain active low configuration. These pins may be used for DMA and modem control. **BRG – Baud Rate Generator** – Operates from the oscillator or external clock input and is capable of generating 27 commonly used data communications baud rates ranging from 50 to 38.4K baud. Programming bit 0 of MR0 to a “1” gives additional baud rates to 230.4kB. These will be in the 16X mode. A 3.6864MHz crystal or external clock must be used to get the standard baud rates. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or external timing signal. **Counter-Timer** – A programmable 16–bit divider that is used for generating miscellaneous clocks or generating timeout periods. These clocks may be used by any or all of the receivers and transmitters in the DUART or may be directed to an I/O pin for miscellaneous use. For Counter – Timer programming, please refer to the D2692’s user manual. **Input Port** – The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address H’D’. A High input results in logic 1 while a Low input results in logic 0. D7 will always read as logic 1. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic or modem and DMA control. Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1 and IP0. A High-to-Low or Low-to-High transition of these inputs will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change-of-state can also be programmed to generate an interrupt to the CPU. **Output Port** – The output ports are controlled from five places: the OPCR register, SOPR, ROPR, the MR registers and the command register (CR). The OPCR register controls the source of the data for the output ports OP2 through OP7. The data source for output ports OP0 and OP1 is controlled by the MR and CR registers. Normally the data source for the OP pins is from the OPR register. The OP pin drives the inverted level (complement) of the OPR register. Example: when the SOPR is used to set the OPR bit to a logical 1 then the associated OP pin will drive a logical 0. The content of the OPR register is controlled by the “Set Output Port Bits Command” and the “Reset Output Bits Command”. These commands are at E and F, respectively. When these commands are used, action takes place only at the bit locations where ones exist. For example, a one in bit location 5 of the data word used with the “Set Output Port Bits” command will result in OPR(5) being set to one. The OP5 would then be set to Low State. Similarly, a one in bit position 5 of the data word associated with the “Reset Output Ports Bits” command would set OPR(5) to zero and, hence, the pin OP5 to a High State. Please note that these pins drive both high and low. However when they are programmed to represent interrupt type functions (such as RxRDY) they will be switched to an open drain configuration.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in Table 1. The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and

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transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped. Each channel has 3 mode registers (MR0, 1, 2) which control the basic configuration of the channel. Access to these registers is controlled by independent MR address pointers. These pointers are set to 0 or 1 by MR control commands in the command register “Miscellaneous Commands”. Each time the MR registers are accessed the MR pointer increments, stopping at MR2. It remains pointing to MR2 until set to 0 or 1 via the miscellaneous commands of the command register. The pointer is set to 1 on reset for compatibility with previous Philips Semiconductors UART software. Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to Table 2 for register bit descriptions. The reserved registers at addresses H‘02’ and H‘0A’ should never be read during normal operation since they are reserved for internal diagnostics.

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA** devices after Place & Route:

Device	LE/ALM	Memory Bits	F_{max}
ARIA GX	1 063 / 465	304	150 MHz
ARIA V	1 022 / 473	304	174 MHz
CYCLONE2	1 460	304	148 MHz
CYCLONE3	1 493	304	180 MHz
CYCLONE4	1 492	304	166 MHz
CYCLONE5	1 022 / 465	304	170 MHz
STRATIX2	1 057 / 465	304	212 MHz
STRATIX3	1 031 / 494	304	331 MHz
STRATIX4	1 026 / 527	304	337 MHz
STRATIX5	1 056 / 490	304	339 MHz
STRATIX2 GX	1 057 / 465	304	218 MHz
MAX10	1 456	304	170 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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