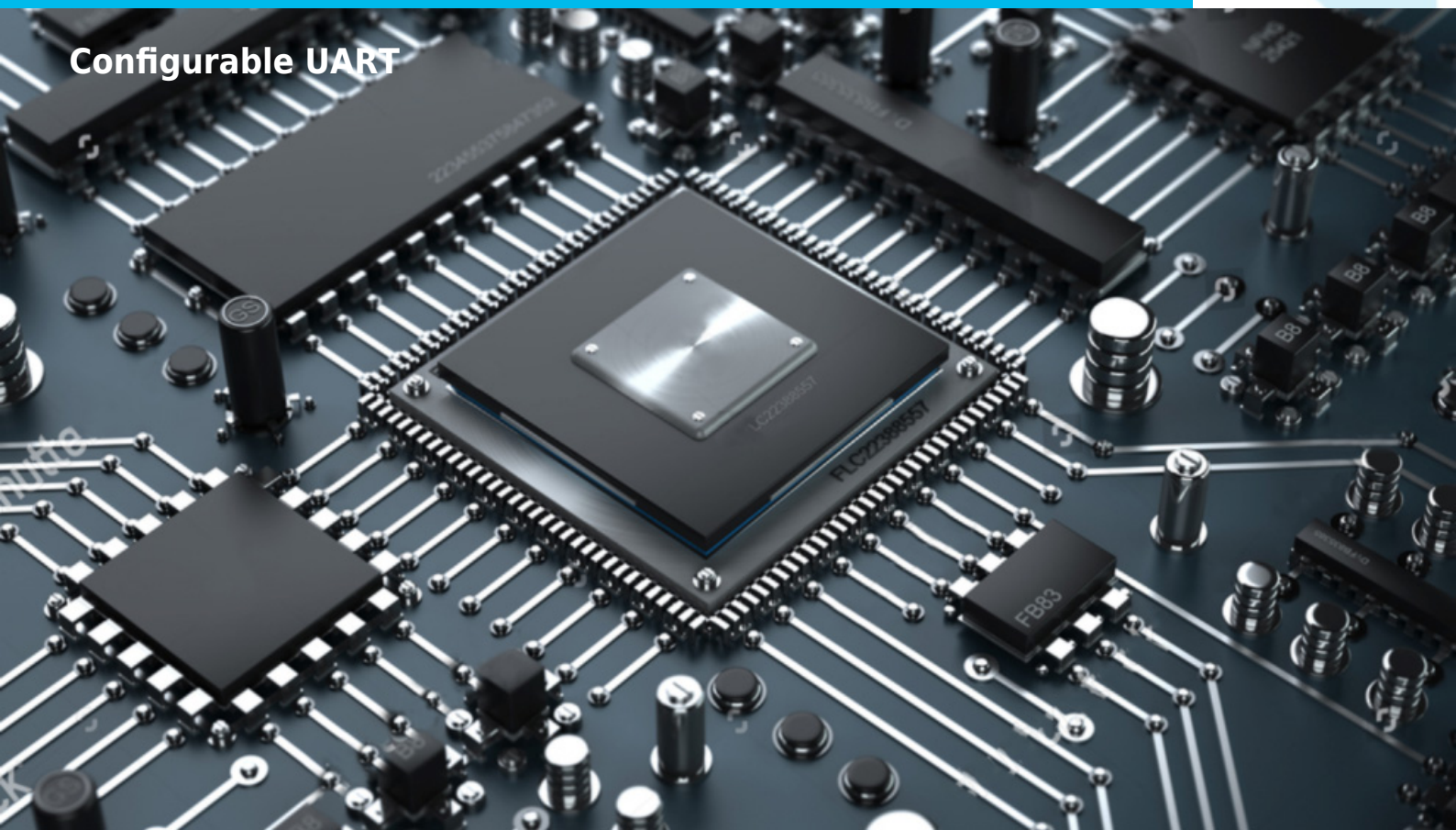
DIGITAL CORE DESIGN

D16450

Configurable UART



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D16450 bridge to APB, AHB, AXI bus, it is a soft core of the Universal Asynchronous Receiver/Transmitter (UART), **functionally identical to the TL16C450**. It performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, but also parallel-to-serial conversion on data characters received from the CPU. The **CPU can read the complete status of the UART at any time** during the functional operation. Reported information status includes the type and condition of transfer operations performed by the UART, as well as any error conditions (parity, overrun, framing or break interrupt). The D16450 includes a **programmable baud rate generator** which is capable of dividing the timing reference clock input by divisors of 1 to (2^{16}-1), and producing a 16 × clock for driving the internal transmitter logic. Provisions are also included to use this 16 × clock to drive receiver logic. Our proprietary solution also has a **complete MODEM control capability** and processor-interrupt system. Interrupts can be programmed according to your requirements, minimizing the computing required to handle the communication link. A separate BAUD CLK line allows setting **an exact transmission speed**, while UART internal logic is clocked with CPU frequency. The core is perfect for applications where the UART core and microcontroller are clocked by the same clock signal and implemented inside the same ASIC or FPGA chip. Our solution is also **dedicated to a standalone implementation**, where several UARTs are required to be implemented inside a single chip and driven by some off-chip devices. Thanks to the D16450 universal interface, both **core implementation and verification are very simple**. They can be simply done by eliminating a number of clock trees in the complete system. The D16450 includes a **fully automated test bench** with a **complete set of tests,** allowing easy package validation at each stage of the SoC design flow. Our trustworthy solution is a technology-independent design, which can be implemented in a variety of process technologies.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- Software compatible with 16450 UART
- **Configuration capability**
- **Separate configurable BAUD clock line**
- Majority Voting Logic
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1,5-, or 2-stop bit generation
  - Internal baud generator
- Complete status reporting capabilities
- Line break generation and detection. Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**
- Fully synthesizable
- Static synchronous design and no internal tri-states

DESIGN FEATURES

The functionality of the D16450 core was based on the Texas Instruments' TL16C450. The following characteristics differentiate the D16450 from Texas Instruments' devices:

- The bi-directional data bus has been split into two separate buses: datai(7:0), datao(7:0)
- Signals rd2 and wr2, xin, and xout have been removed from interface
- Signal ADS and address latch have been removed
- The DLL, DLM and THR registers are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge, following a THR write
- RCLK clock is replaced by global clock CLK, internally divided by BAUD factor.
- Asynchronous microcontroller interface is replaced by

equivalent Universal interface
- All latches implemented in original 16450 devices are replaced by equivalent flip-flop registers with the same functionality

UNITS SUMMARY

Data Bus Buffer – Accepts inputs from the system bus and generates control signals for other D14750 functional blocks. Address bus ADDR(2:0) selects one of the registers to be read from/written into. Both RD and WE signals are active low and are qualified by CS; RD and WE are ignored unless the D16450 has been selected by holding CS low.
Baud Generator – Divides clock input by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16 × the baud rate. Two 8-bit registers called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16450 in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM to prevent long counts on initial load.
Modem Control Logic – Controls an interface with the MODEM or data set (or a peripheral device emulating a MODEM).
Interrupt Controller – Controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Identification (IIR) registers.
Receiver Control – The receiving starts, when the falling edge on Serial Input (SI) during IDLE State is detected. After starting the SI input is sampled every 16 internal baud cycles, as it is shown in the figure below. When the logic 1 state is detected during START bit, it means, that the False Start bit was detected and receiver back to the IDLE state.
Transmitter Control – Controls transmission of written to THR (Transmitter Holding register) character via serial output SO. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

CONFIGURATION

The following parameters of the D16450 core can be easy adjusted to requirements of dedicated application and technology. Core configuration can be prepared by effortless changing appropriate constants in package file. There is no need to change any part of the code.

- Baud generator: *enable / disable*
- External RCLK source: *enable / disable*
- External BAUDCLK source: *enable / disable*
- Asynchronous input buffer: *enable / disable*
- Modem Control: *enable / disable*
- SCR register: *enable / disable*

PERFORMANCE

The following table gives a survey about the Core area and performance in **LATTICE®** devices, after Place & Route (all key features included):

Device	Speed grade	LUTs/PFUs	F_{max}
SC	-7	346 / 164	220 MHz
ECP2	-7	341 / 164	198 MHz
ECP2M	-7	285 / 160	198 MHz
XP2	-7	285 / 160	137 MHz
XP	-5	389 / 182	124 MHz
ECP	-5	389 / 182	135 MHz
EC	-5	389 / 182	146 MHz
ORCA 4	-3	310 / 57	80 MHz
ORCA 3	-7	299 / 57	47 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited.

There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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