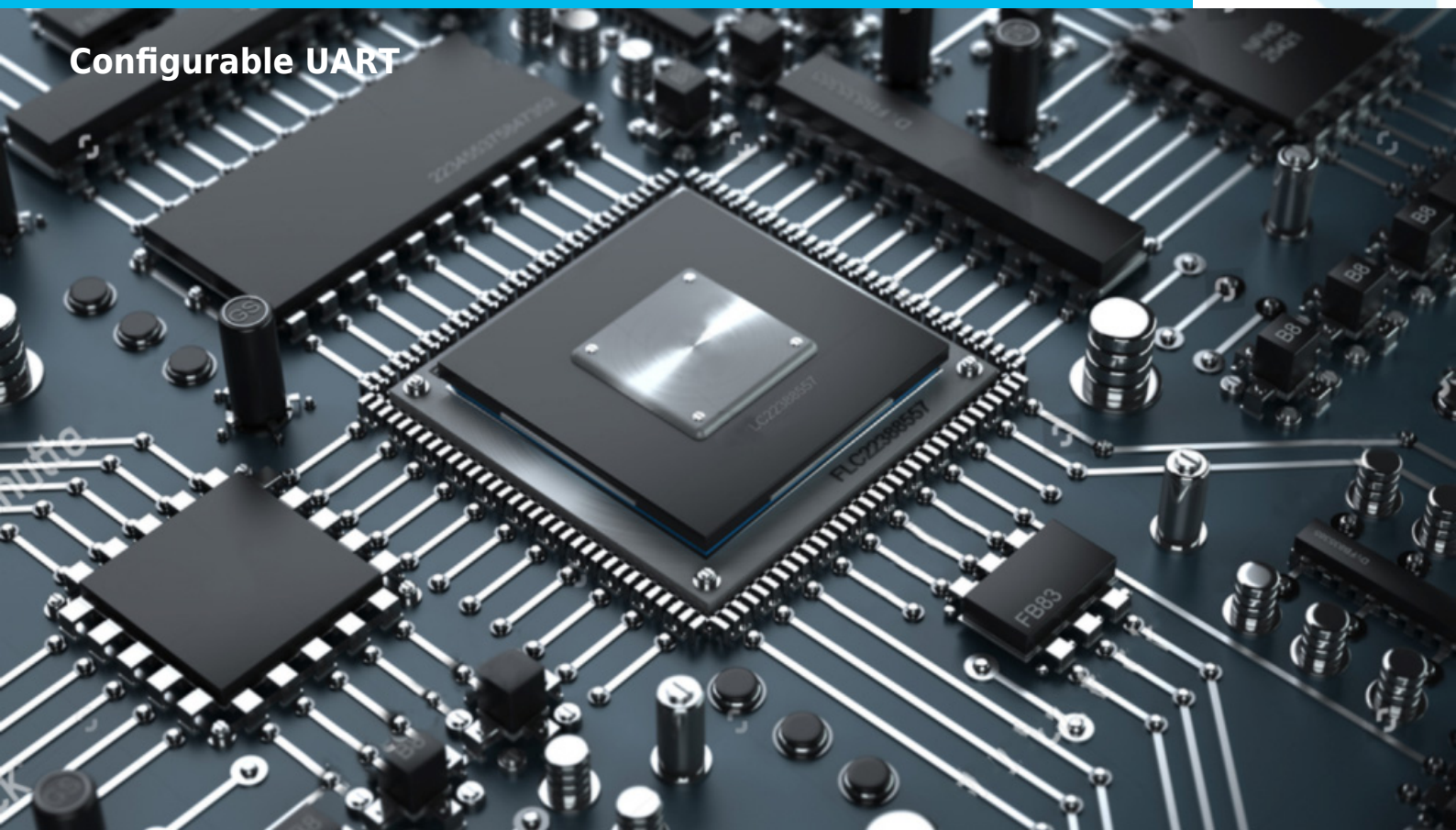
DIGITAL CORE DESIGN

D16450

Configurable UART



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D16450 UART IP Core – Classic Asynchronous UART for FPGA & ASIC

The **D16450 UART IP Core** from **DCD-SEMI** is a compact and reliable **Universal Asynchronous Receiver/Transmitter (UART)** designed for **FPGA and ASIC integration**. Delivered as a flexible **bridge to APB, AHB, and AXI bus architectures**, the D16450 is **functionally identical to the TL16C450**, ensuring full compatibility with legacy software and hardware environments.

The core performs **serial-to-parallel conversion** for data received from peripherals or MODEMs and **parallel-to-serial conversion** for data transmitted from the CPU, providing a proven and deterministic UART implementation for embedded systems.

Complete Status Visibility and Error Reporting

The processor can read the **full UART status at any time** during operation. Status information includes:

- Current transfer operation state
- **Parity, overrun, framing, and break error detection**
- Interrupt source identification

This comprehensive reporting ensures predictable communication behavior and simplifies software development and debugging.

Programmable Baud Rate and Flexible Clocking

The D16450 integrates a **programmable baud rate generator** capable of dividing a reference clock by divisors from **1 to ($2^{16} - 1$)**, generating a **16× clock** for the internal transmitter logic. The same clock can also be used to drive the receiver logic.

A dedicated **BAUD CLK input** allows designers to set an **exact transmission speed**, while the UART internal logic continues to operate at the CPU clock frequency. This separation simplifies timing closure and improves design robustness.

MODEM Control and Interrupt-Driven Operation

The core includes **full MODEM control capability** and a **programmable processor interrupt system**, allowing efficient, interrupt-driven communication. Interrupts can be tailored to application requirements, minimizing CPU overhead and eliminating unnecessary polling.

Optimized for SoC and Multi-UART Designs

The D16450 is ideal for systems where the **UART and microcontroller share the same clock domain** inside a single FPGA or ASIC. Its **universal interface** reduces clock-tree complexity and significantly simplifies both **implementation and verification**.

The core is also well suited for **standalone multi-UART designs**, where several UART instances are implemented within one chip and connected to off-chip devices.

Verification-Ready and Technology Independent

Like all DCD-SEMI UART IP Cores, the D16450 is delivered with a **fully automated testbench and complete test suite**, enabling straightforward validation throughout every stage of the **SoC design flow**.

The IP Core is **technology-independent** and can be implemented across a wide range of **FPGA and ASIC process technologies**.

Typical Applications

- Legacy UART replacement
- Embedded controllers and SoCs
- Industrial and instrumentation systems
- FPGA-based multi-UART designs
- ASIC designs requiring deterministic serial communication

Which UART IP Core Should You Choose?

Choosing the right UART IP Core depends on **software compatibility**, **throughput requirements**, and **CPU load constraints**. DCD-SEMI offers three UART solutions covering classic legacy replacement up to high-performance designs.

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Quick Decision Guide

Choose D16450 if:

- You are replacing a **TL16C450 / 16450 UART**
- You need **100% register compatibility**
- Minimal validation effort is critical

Choose D16550 if:

- You need **FIFO buffering** but still want classic UART behavior
- You are migrating from **16550-based systems**
- Moderate throughput improvement is required

Choose D16950 if:

- You need **maximum throughput and lowest CPU load**
- Large FIFO depth and advanced flow control are required
- You are upgrading legacy UARTs in performance-critical systems

Feature Comparison Table

Feature	D16450	D16550	D16950
Legacy Compatibility	16450 / TL16C450	16550 / 16550A	16450–16750 + OX16C950
FIFO Support	□ No FIFO	□ 16-byte FIFO	□ 128-byte FIFO
FIFO Trigger Levels	—	Fixed	Programmable (1–127)
CPU Load	High	Medium	Low
Max Throughput	Low–Medium	Medium	High
Flow Control (RTS/CTS)	Basic	Basic	Advanced autoflow
9-bit Mode	□	□	□
Synchronous Mode	□	□	□
MODEM Control	Full	Full	Full
Interrupt System	Programmable	Programmable	Advanced programmable
External Clock Sync	□	□	□
Bus Interfaces	APB / AHB / AXI	APB / AHB / AXI	APB / AHB / AXI
Technology Independent	□	□	□
Typical Use Case	Drop-in legacy replacement	FIFO-based legacy upgrade	High-performance UART

Engineering Trade-Offs Explained

D16450 – Lowest Risk Legacy Replacement

- Exact behavior match to legacy hardware
- No FIFO → deterministic timing
- Best choice when **software must remain untouched**

Best for: industrial legacy systems, PC-compatible UART emulation

D16550 – Balanced Upgrade Path

- Adds FIFO buffering to reduce interrupts
- Still widely supported by legacy drivers
- Good compromise between compatibility and performance

Best for: embedded Linux, RTOS-based systems

D16950 – Performance-Oriented Modern UART

- Deep FIFOs dramatically reduce CPU overhead
- Autoflow control prevents data loss at high speeds
- Supports multi-UART SoCs and clock-synchronous designs

Best for: telecom, industrial gateways, FPGA-based SoCs

Migration Scenarios

Migrating from Discrete UART ICs to FPGA/ASIC

- **16450 IC → D16450** (no software changes)
- **16550 IC → D16550** (minimal validation)
- **OX16C950 → D16950** (performance parity or better)

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Selection Summary

Project Priority	Recommended IP
Zero software changes	**D16450**
Moderate CPU optimization	**D16550**
Maximum performance	**D16950**

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

DESIGN FEATURES

The functionality of the D16450 core was based on the Texas Instruments' TL16C450. The following characteristics differentiate the D16450 from Texas Instruments' devices:

- The bi-directional data bus has been split into two separate buses: datai(7:0), datao(7:0)
- Signals rd2 and wr2, xin, and xout have been removed from interface
- Signal ADS and address latch have been removed
- The DLL, DLM and THR registers are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge, following a THR write
- RCLK clock is replaced by global clock CLK, internally divided by BAUD factor.
- Asynchronous microcontroller interface is replaced by equivalent Universal interface
- All latches implemented in original 16450 devices are replaced by equivalent flip-flop registers with the same functionality

UNITS SUMMARY

Data Bus Buffer – Accepts inputs from the system bus and generates control signals for other D14750 functional blocks. Address bus ADDR(2:0) selects one of the registers to be read from/written into. Both RD and WE signals are active low and are qualified by CS; RD and WE are ignored unless the D16450 has been selected by holding CS low.
Baud Generator – Divides clock input by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16 × the baud rate. Two 8-bit registers called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16450 in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM to prevent long counts on initial load.
Modem Control Logic – Controls an interface with the MODEM or data set (or a peripheral device emulating a MODEM).
Interrupt Controller – Controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Identification (IIR) registers.
Receiver Control – The receiving starts, when the falling edge on Serial Input (SI) during IDLE State is detected. After starting the SI input is sampled every 16 internal baud cycles, as it is shown in the figure below. When the logic 1 state is detected during START bit, it means, that the False Start bit was detected and receiver back to the IDLE state.
Transmitter Control – Controls transmission of written to THR (Transmitter Holding register) character via serial output SO. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.

CONFIGURATION

The following parameters of the D16450 core can be easy adjusted to requirements of dedicated application and technology. Core configuration can be prepared by effortless changing appropriate constants in package file. There is no need to change any part of the code.

- Baud generator: *enable / disable*
- External RCLK source: *enable / disable*
- External BAUDCLK source: *enable / disable*
- Asynchronous input buffer: *enable / disable*
- Modem Control: *enable / disable*
- SCR register: *enable / disable*

PERFORMANCE

The following table gives a survey about the Core area and performance in **LATTICE FPGA** devices, after Place & Route (all key features included):

Device	Speed grade	LUTs/PFUs	F_{max}
SC	-7	346 / 164	220 MHz
ECP2	-7	341 / 164	198 MHz
ECP2M	-7	285 / 160	198 MHz
XP2	-7	285 / 160	137 MHz
XP	-5	389 / 182	124 MHz
ECP	-5	389 / 182	135 MHz
EC	-5	389 / 182	146 MHz
ORCA 4	-3	310 / 57	80 MHz
ORCA 3	-7	299 / 57	47 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

APPLICATIONS

- Serial Data communications applications
- Modem interface

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- Embedded microprocessor boards

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited.

There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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