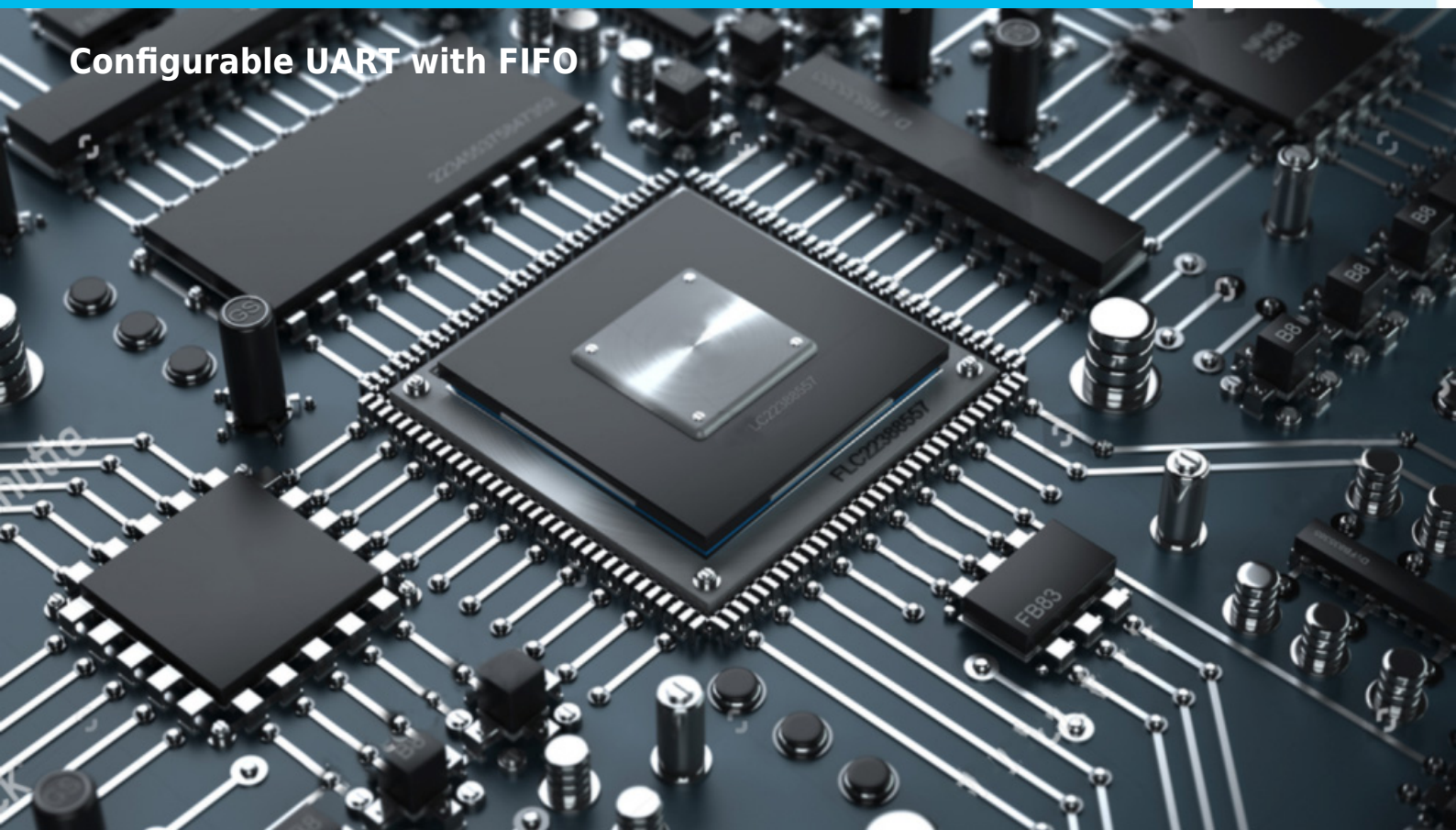
DIGITAL CORE DESIGN

D16550

Configurable UART with FIFO



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D16550 bridge to APB, AHB, AXI bus, it is a soft Core of Universal Asynchronous Receiver/Transmitter (UART), **functionally identical to the TL16C550A**. It **allows serial transmission in two modes – UART and FIFO**. In the FIFO mode, internal FIFOs are activated allowing 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both, receive and transmit directions. The D16550 **performs serial-to-parallel conversion on data characters** received from a peripheral device or MODEM, and parallel-to-serial conversion on data characters received from the CPU. The **CPU can read the complete status of the UART at any time** during the functional operation. Reported status information includes the type and condition of transfer operations performed by the UART, as well as any error conditions (parity, overrun, framing or break interrupt). The D16550 includes a **programmable baud rate generator**, which is capable of dividing a timing reference clock input by divisors of 1 to (2^{16}-1) and producing a 16 × clock for driving internal transmitter logic. Provisions are also included to use this 16 × clock to drive receiver logic. Our softcore incorporates **complete MODEM control capability and a processor-interrupt system**. What's more important, interrupts can be programmed to your requirements, minimizing the computing required to handle the communication link. A separate BAUD CLK line allows setting **an exact transmission speed**, while UART internal logic is clocked with CPU frequency. During the Synthesis process, configuration capability allows you to enable or disable Modem Control Logic and FIFOs, or change the FIFO's size. So, in applications with area limitation and where the UART works only in the 16450 modes, disabling Modem Control and FIFOs **allow to save about 50% of logic resources**. Our trustworthy Core is perfect for applications where the UART core and microcontroller are clocked by the same clock signal and are implemented inside the same ASIC or FPGA chip. We recommend it also for a standalone implementation, where several UARTs are required to be implemented inside a single chip and driven by some off-chip devices. Thanks to a universal interface, the D16550 core implementation and verification are very simple, just by eliminating a number of clock trees in the complete system. The D16550 includes **a fully automated test bench** with a **complete set of tests,** allowing easy package validation at each stage of the SoC design flow. Please remember that our softcore is a technology-independent design, so can be implemented in a variety of process technologies.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.

- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

KEY FEATURES

- Software compatible with 16450 and 16550 UARTs
- **Configuration capability**
- **Separate configurable BAUD clock line**
- Majority Voting Logic
- Two modes of operation: UART mode and FIFO mode
  - In the FIFO mode transmitter and receiver are each buffered with 16 byte FIFO to reduce the number of interrupts presented to the CPU
  - In UART mode receiver and transmitter are double buffered to eliminate a need for precise synchronization between the CPU and serial data
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Fully programmable serial interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd or no-parity bit generation and detection
  - 1-, 1 ½-, or 2-stop bit generation
  - Internal baud generator
- Complete status reporting capabilities
- Line break generation and detection. Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**
- Fully synthesizable

- Static synchronous design and no internal tri-states

OPTIONAL FEATURES

- **RS232 and RS485 standards support**
- IEEE 1284 Bidirectional Parallel Data Port
- Compatible with Standard Centronics Parallel Interface
- Support for Parallel Protocols: ECP and EPP
- Decompression of Run Length Encoded Data in ECP Reserve Mode
- Serial Ports with Infrared Data Association (IRDA) inputs and outputs

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

DESIGN FEATURES

The functionality of the D16550 core was based on the Texas Instruments' TL16C550A. The following characteristics differentiate the D16550 from Texas Instruments' devices:

- The bi-directional data bus have been split into two separate buses: datai (7:0), datao (7:0)
- Signals rd2 and wr2, xin and xout have been removed from interface
- Signal ADS and address latch have been removed
- The DLL, DLM and THR registers are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge following a THR write
- RCLK clock is replaced by global clock CLK, internally divided by BAUD factor.
- Asynchronous microcontroller interface is replaced by equivalent Universal interface
- All latches implemented in original 16550 devices are replaced by equivalent flip-flop registers, with the same functionality

UNITS SUMMARY

Baud Generator – The D16550 contains a programmable 16 bit baud generator that divides clock input by a divisor in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16 × the baud rate. Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16550, in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM, to prevent long counts on initial load.
Data Bus Buffer – The data Bus Buffer accepts inputs from the system bus and generates control signals for other D16550 functional blocks. Address bus ADDR(2:0) selects one of the registers to be read from/written into. Both, RD and WE signals, are active low and are qualified by CS; RD and WE are ignored, unless the D16550 has been selected by holding CS low.
Modem Control Logic controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).
Interrupt Controller – D16550 contains fully prioritized interrupt system controller. It controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Identification (IIR) registers.
Receiver Control – Receiving starts, when the falling edge on Serial Input (SI) during IDLE State is detected. After starting, the SI input is sampled every 16 internal baud cycles, as it is shown in figure above. When the logic 1 state is detected during START bit, it means, that the False Start bit was detected and receiver is back to the IDLE state.
Receiver FIFO – The Rx FIFO is 16 levels deep, it receives data, until the number of bytes in the FIFO, equals the selected interrupt trigger level. At that time, if R x interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes, until it holds 16 of them. It will not accept any more data, once it is full. Any more data entering the Rx shift register will set the Overrun Error flag.
Transmitter Control module controls transmission of written to THR (Transmitter Holding register) character via serial output SO. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.
Transmitter FIFO – the T x portion of the UART, transmits data through SO as soon as the CPU loads a byte into the T x FIFO. The UART will prevent loads to the T x FIFO, if it currently holds 16 characters. Loading to the T x FIFO will again be enabled, as soon as the next character is transferred to the T x shift register. These capabilities account for the largely autonomous operation of the T x. The UART starts the above operations typically with a T x interrupt.

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CONFIGURATION

The following parameters of the D16550 core can be easily

adjusted to the requirements of dedicated application and technology. Core configuration can be effortlessly done, by changing appropriate constants in package file. There is no need to change any part of the code.

- Baud generator: *enable / disable*
- External RCLK source: *enable / disable*
- External BAUDCLK source: *enable / disable*
- Asynchronous input buffer: *enable / disable*
- Modem Control: *enable / disable*
- SCR register: *enable / disable*
- FIFO Control logic: *enable / disable*
- FIFO's size: *2 / 4 / 8 / 16 – default*

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	LE/ALM	Memory Bits	F_{max}
ARIA GX	342/231	304	243 MHz
ARIA V	330/263	304	209 MHz
CYCLONE	465	304	193 MHz
CYCLONE2	476	304	220 MHz
CYCLONE3	477	304	250 MHz
CYCLONE4	478	304	250 MHz
CYCLONE5	328/231	304	187 MHz
STRATIX	465	304	206 MHz
STRATIX2	342/232	304	343 MHz
STRATIX3	334/231	304	527 MHz
STRATIX4	330/250	304	497 MHz
STRATIX5	332/262	304	456 MHz
STRATIX GX	465	304	214 MHz
STRATIX2 GX	340/231	304	341 MHz
MAX10	432	304	181 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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