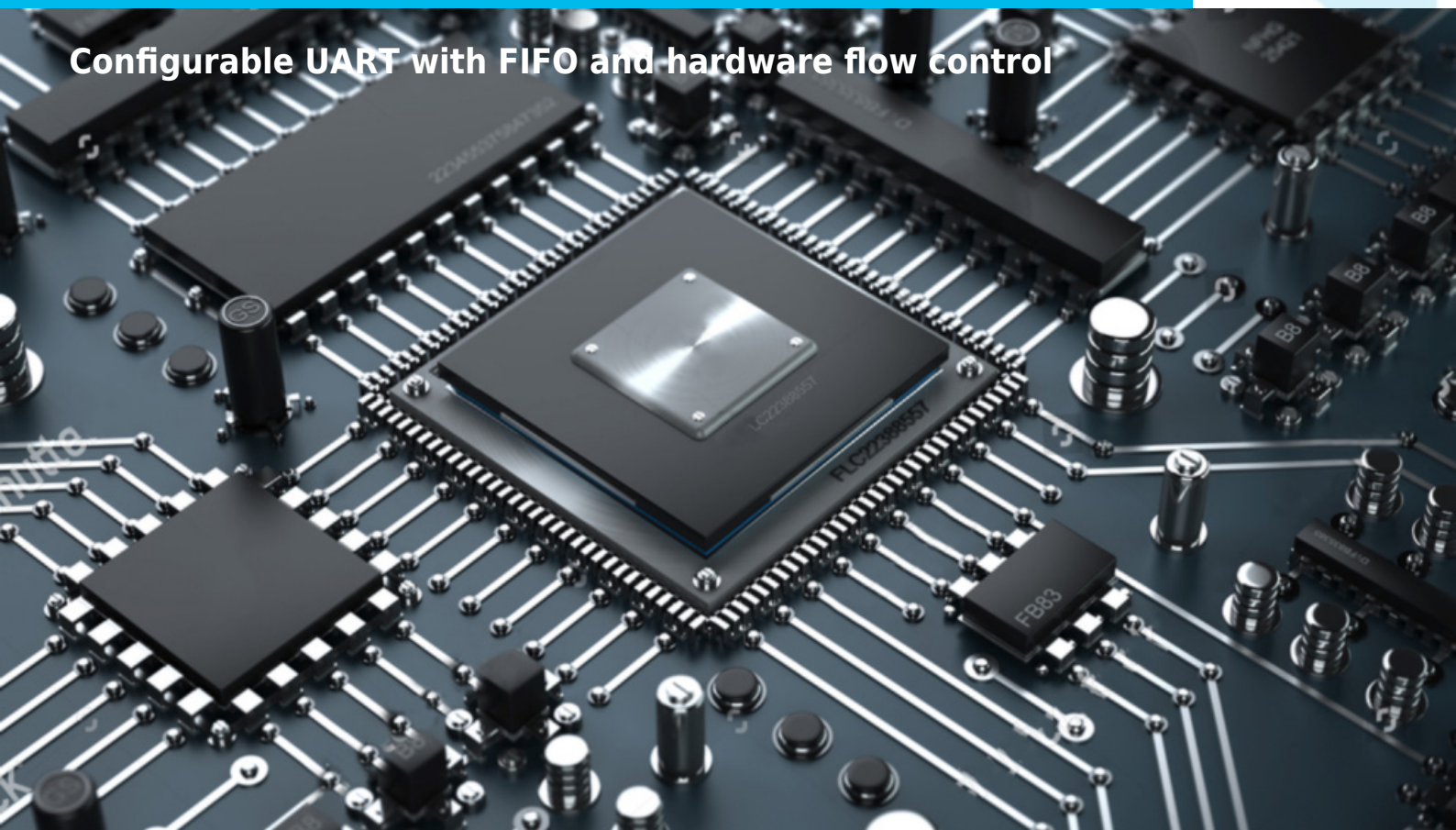
DIGITAL CORE DESIGN

D16750

Configurable UART with FIFO and hardware flow control



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D16750 bridge to APB, AHB, AXI bus, it is a soft Core of a Universal Asynchronous Receiver / Transmitter (UART), **functionally identical to the TL16C750**. The D16750 allows **serial transmission in two modes – UART and FIFO**. In the FIFO mode, internal FIFOs are activated allowing up to 512 bytes (plus 3 bits data error per byte in the RCVR FIFO) to be stored both in receive and transmit directions. Our trustworthy core performs serial-to-parallel conversion on data characters received from a peripheral device or from MODEM, and a parallel-to-serial conversion on data characters received from the CPU. The **CPU can read a complete status of the UART at any time** during functional operation. Reported status information includes a type and condition of transfer operations performed by the UART, as well as any error conditions (parity, overrun, framing or break interrupt). The D16750 includes a programmable baud rate generator, which is capable of dividing the timing reference clock input by divisors of 1 to (216-1) and producing a 16 × clock for driving internal transmitter logic. Provisions are also included to use this 16 × clock to drive receiver logic. What's more important, our revolutionary **core has a complete MODEM control capability** and processor-interrupt system. Thanks to it, interrupts can be programmed in accordance to your requirements, minimizing the computing required to handle the communication link. A separate BAUD CLK line allows to set an exact transmission speed, while the UART internal logic is clocked with CPU frequency. The **configuration capability allows you to enable or disable the Modem Control Logic and FIFO's, or change the FIFO's size during the Synthesis process**. So, in applications with area limitation and where the UART works only in the 16450 mode, disabling Modem Control and FIFO's allow saving about 50% of logic resources. The core is perfect for applications where the UART Core and microcontroller are clocked by the same clock signal and are implemented inside the same ASIC or FPGA chip, as well as for standalone implementation, where several UARTs are required to be implemented inside a single chip and driven by some off-chip devices. Thanks to a universal interface, the **D16750 core implementation and verification are very simple**, just by eliminating a number of clock trees in the complete system. Moreover, we have implemented a selectable autoflow control feature in the FIFO mode. What does it mean for you? Thanks to this useful feature, you can significantly reduce software overload and increase system efficiency. It'll be **done automatically by controlling serial data flow through the RTS output and the CTS input signals**. The D16750 includes **fully automated test bench** with **complete set of tests,** allowing easy package validation at each stage of SoC design flow. Our core is a technology independent design, which can be implemented in variety of process technologies.

KEY FEATURES

- Software compatible with 16450, 16550 and 16750 UARTs
- **Configuration capability**
- **Separate configurable BAUD clock line**
- Majority Voting Logic
- **Supports RS232 and RS485 standards**
- Two modes of operation: UART mode and FIFO mode
  - In the FIFO mode transmitter and receiver are each buffered with 64 byte FIFO to reduce the number of interrupts presented to the CPU
  - In UART mode receiver and transmitter are double buffered to eliminate a need for precise synchronization between the CPU and serial data
- Configurable **FIFO size** allowing **up to 512 levels** deep FIFOs in both Rx and Tx directions.
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI & DCD)
- Programmable automatic Hardware Flow Control logic through Auto-RTS and Auto-CTS
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1.5-, or 2-stop bit generation
  - Internal baud generator
- Complete status reporting capabilities
- Line break generation and detection. Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**
- Fully synthesizable

OPTIONAL FEATURES

- IEEE 1284 Bidirectional Parallel Data Port
- Compatible with Standard Centronics Parallel Interface
- Support for Parallel Protocols: ECP and EPP
- Decompression of Run Length Encoded Data in ECP Reserve Mode
- Serial Ports with Infrared Data Association (IRDA) inputs and outputs

DESIGN FEATURES

The functionality of the D16750 core was based on the Texas Instruments' TL16C750A. The following characteristics differentiate the D16750 from Texas Instruments' devices:

- The bi-directional data bus has been split into two separate buses: datai (7:0), datao (7:0)
- Signals rd2 and wr2, x in, and x out have been removed from interface
- The DLL, DLM and THR registers are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge following a THR write
- RCLK clock is replaced by global clock CLK, internally divided by BAUD factor.
- Asynchronous microcontroller interface is replaced by equivalent Universal interface
- All latches implemented in original 16750 devices, are replaced by equivalent flip-flop registers, with the same functionality

UNITS SUMMARY

Baud Generator – The D16750 contains a programmable 16 bit baud generator that divides clock input by a divisor, in the range between 1 and (2^{16}–1). The output frequency of the baud generator is 16 × the baud rate. Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16750, in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM, to prevent long counts on initial load.
Data Bus Buffer – Accepts inputs from a system bus and generates control signals for other D16750 functional blocks. Address bus ADDR (2:0) selects one of registers to be read from/written into. Both RD and WE signals are active low and are qualified by CS; RD and WE are ignored, unless the D16750 has been selected by holding CS low.
Modem Control Logic – Controls an interface with the MODEM or data set (or a peripheral device emulating a MODEM).
Interrupt Controller – D16750 contains fully prioritized interrupt system controller which controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Identification (IIR) registers.
Receiver Control – Receiving starts, when the falling edge on Serial Input (SI) during IDLE State is detected. After starting, the SI input is sampled every 16 internal baud cycles, as it is shown in figure above. When the logic 1 state is detected during START bit, it means that the False Start bit was detected and receiver is back to the IDLE state.
Receiver FIFO – The R x FIFO can be 64 (128, 256, 512) levels deep, it receives data, until the number of bytes in the FIFO, equals the selected interrupt trigger level. At that time, if R x interrupts are enabled, the UART will issue an interrupt to the CPU. The R x FIFO will continue to store bytes, until it is full and will not accept any further bytes. Any more data entering the R x shift register will set the Overrun Error flag.
Transmitter Control module – Controls transmission of written to THR (Transmitter Holding register) character via serial output SO. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.
Transmitter FIFO – the T x portion of the UART, transmits data through SO as soon, as the CPU loads a byte into the T x FIFO. The UART will prevent loads to the T x FIFO, if it currently holds 64 (128, 256, 512) characters (depending on FCR (5) bit value and selected FIFO size). Loading to the T x FIFO will be enabled again, as soon as the next character is transferred to the T x shift register. These capabilities account for the largely autonomous operation of the T x. The UART starts above operations typically with a T x interrupt.

CONFIGURATION

The following parameters of the D16750 core can be easy adjusted to requirements of proprietary application and technology. Core configuration can be effortlessly done by changing appropriate constants in package file. There is no need to change any part of the code.

- Baud generator: *enable / disable*
- External RCLK source: *enable / disable*
- External BAUDCLK source: *enable / disable*
- Modem Control: *enable / disable*
- SCR register: *enable / disable*
- FIFO Control logic: *enable / disable*
- FIFO Size: *normal 16/64 / large, up to 512*

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	LE/ALM	Memory Bits	F_{max}
ARIA GX	381/243	1 216	228 MHz
ARIA V	365/283	1 216	214 MHz
CYCLONE	488	1 216	170 MHz
CYCLONE2	496	1 216	197 MHz
CYCLONE3	498	1 216	247 MHz
CYCLONE4	495	1 216	250 MHz
CYCLONE5	365/243	1 216	188 MHz
STRATIX	488	1 216	180 MHz
STRATIX2	382/245	1 216	333 MHz
STRATIX3	382/297	1 216	454 MHz
STRATIX4	369/263	1 216	457 MHz
STRATIX5	367/282	1 216	400 MHz

STRATIX GX	488	1 216	185 MHz
STRATIX2 GX	380/244	1 216	317 MHz
MAX10	473	1 216	188 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Multi-Site license option* – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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