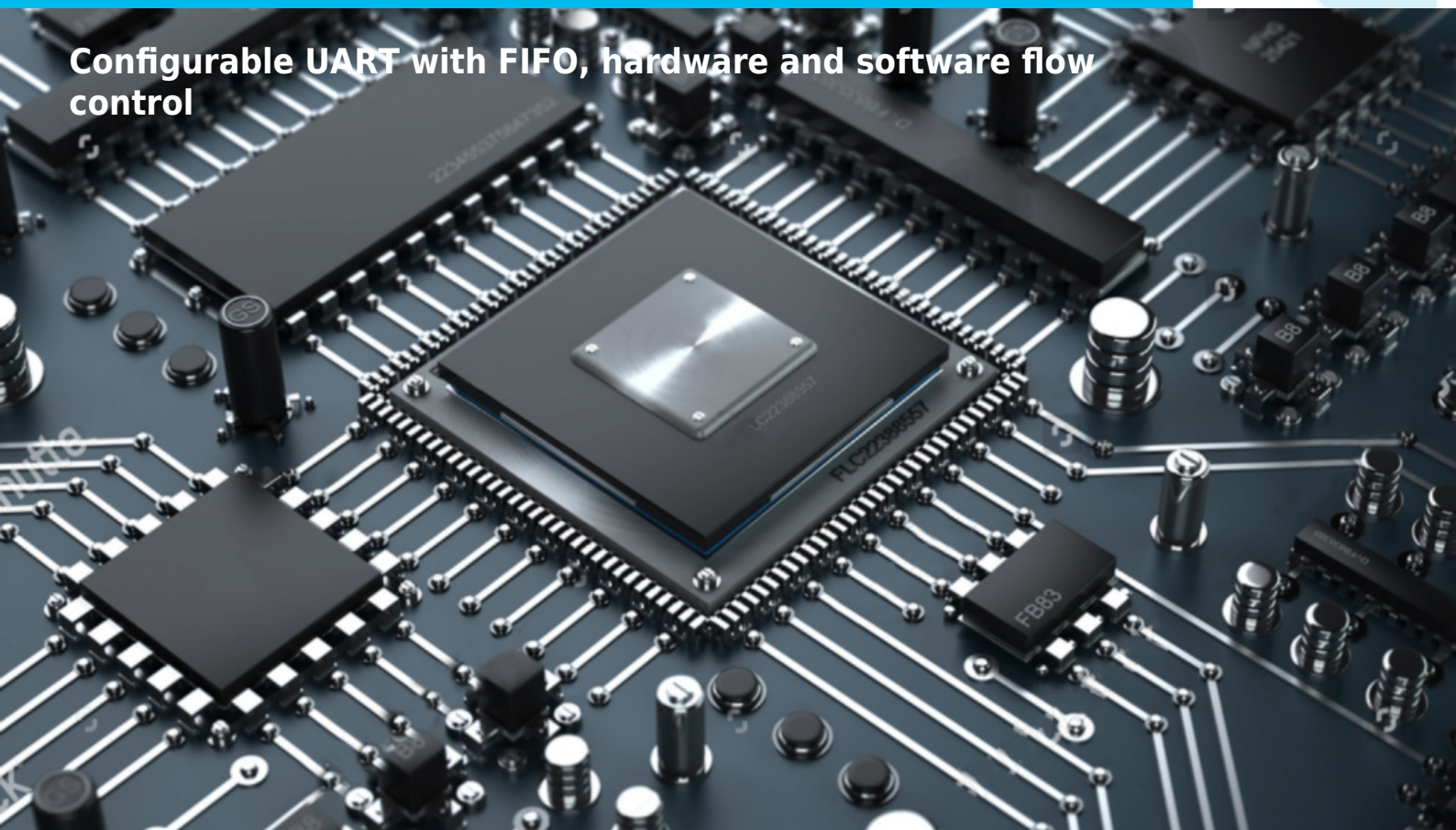
DIGITAL CORE DESIGN

D16752

Configurable UART with FIFO, hardware and software flow control



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D16752 is a universal asynchronous receiver/transmitter (UART) with **64-byte FIFOs and automatic hardware/software flow control**. It offers **enhanced features**, like transmission control register (TCR) which stores received FIFO threshold level in order to start/stop transmission during hardware and sofware flow control. With the FIFO RDY register, the software gets a status of TXRDY/RXRDY for all UART ports in one access. **On board status registers** provide you with error indications and operational status modem interface control. System interrupts may be tailored to meet your requirements. An internal loop back capability allows on board diagnostics. The UART transmits data sent to it from a peripheral 8-bit bus on TX signal and receives characters on a RX signal. Characters can be programmed to be 5, 6, 7 or 8 bits. The UART has a 64-byte receive FIFO and transmit FIFO, which can be programmed to interrupt at different trigger levels. The UART generates its own desired baud rate based upon a programmable divisor and its input clock. It can **transmit even, odd or no parity and 1, 1.5, or 2 stop bits**. The receiver can detect break, idle or framing errors, FIFO overflow and parity errors. On the other hand, the transmitter can detect a FIFO underflow. The UART also contains a software interface for modem control operations and has a software flow control combined with hardware flow control capabilities. **The D16752 is software compatible with the TL16C752**. It **provides few enhanced features**, which are provided through a special enhanced feature register. The UART will perform a serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-parallel conversion on data characters transmitted by the processor. A complete status of each channel of the D16752 can be read by the CPU at any time during functional operation. Our efficient **core can be placed in an alternate mode** (FIFO mode), relieving the processor of excessive software overhead which is run by buffering received/transmitted characters. Both, the receiver and the transmitter FIFOs, can store up to 64 bytes (including three additional bits of error status per byte for the receiver FIFO) and have selectable or programmable trigger levels. Primary outputs RXRDY and TXRDY allow signalling of DMA transfers. The D16752 has a **selectable hardware flow control and software flow control**. The **hardware flow control** significantly reduces software overhead and increases system efficiency, by automatically controlled serial data flow using the RTS output and CTS input signals. The **Software flow control** automatically monitors data flow by using programmable Xon/Xoff characters. The UART includes a programmable baud rate generator which can divide the timing reference clock input by a divisor between 1 and (216–1). A **separate BAUD CLK** line allows to set an exact transmission speed while UART internal logic is clocked with the CPU frequency. The D16752 includes **fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of SoC design flow. Our efficient Core is a technology independent design that can be implemented in variety of process technologies. **Configuration capability** allows you to enable or disable the Modem Control Logic and the FIFO's Control Logic as well as change the FIFO size during the Synthesis process. So, in applications with area limitation and where the UART works only in a 16450 mode, disabling the Modem Control and FIFO's allow to save about 50% of logic resources. The Core is perfect for applications where the UART core and microcontroller are clocked by the same clock signal and implemented inside the same ASIC or FPGA chip. Nevertheless, our solution is designed for a standalone implementation where several UARTs are required to be implemented inside a single chip and driven by some off-chip devices. Thanks the D16752, the CPU interface core implementation and verification are very simple, just by eliminating a number of clock trees in the complete system. **The D16752 can operate as a dual channel, as well as single channel UART.**

KEY FEATURES

- Software compatible with 16752 UARTs
- **Configuration capability**
- **Dual channel UART – configurable**
- **Separate configurable BAUD clock line**
- **Supports RS232 and RS485 standards**
- **Hardware/Software Data flow control**
  - Programmable Xon/Xoff characters
  - Programmable AutoRTS, AutoCTS
- **Programmable and selectable Transmit and Receive FIFO Trigger levels for DMA and interrupt generation**
- **Programmable Receive FIFO Trigger Levels for Software/Hardware Flow Control**
- **Software Flow Control Turned OFF, optionally by any Xon Rx Character**
- Software Selectable Baud Rate Generator Prescaleable Clock Rates of 1x and 4x
- **Programmable SLEEP Mode**
- Majority Voting Logic
- Two modes of operation: UART mode and FIFO mode
  - In the FIFO mode transmitter and receiver are each buffered with 64 byte FIFO to reduce the number of interrupts presented to the CPU
  - In UART mode receiver and transmitter are double buffered to eliminate a need for precise synchronization between the CPU and serial data
- Configurable **FIFO size** allowing **up to 512 levels** deep FIFOs in both Rx and Tx directions.

- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial interface characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1.5-, or 2-stop bit generation
  - Internal baud generator
- **Complete status reporting capabilities**
- Line break generation and detection. Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- **Available system interface wrappers:**
  - **AMBA – APB Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**
- Fully synthesizable
- Static synchronous design and no internal tri-states

OPTIONAL FEATURES

- IEEE 1284 Bidirectional Parallel Data Port
  - *Compatible with Standard Centronics Parallel Interface*
  - *Support for Parallel Protocols: ECP and EPP*
  - *Data Path 16/64-Byte FIFO Buffer*
  - *Direct Memory Access (DMA) Transfer*
  - *Decompression of Run Length Encoded Data in ECP Reserve Mode*
  - *Direct Connection to Printer, No External Transceiver is needed*
- Serial Ports with Infrared Data Association (IRDA) inputs and outputs

DESIGN FEATURES

The functionality of the D16752 core was based on the Texas Instruments' TL16C752. The following characteristics differentiate the D16752 from Texas Instruments' devices:

- The bi-directional data bus has been split into two separate buses: datai (7:0), datao (7:0)
- The DLL, DLM and THR registers are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge following a THR write
- Asynchronous microcontroller interface is replaced by equivalent Universal interface
- All latches implemented in original 16752 devices are replaced by equivalent flip-flop registers, with the same functionality

UNITS SUMMARY

Data Bus Buffer – The data Bus Buffer accepts inputs from the system bus and generates control signals for other D16752 functional blocks. Address bus ADDR (2:0) selects one of the register to be read from/written into. Both, RD and WE signals, are active low and are qualified by CSA / CSB; RD and WE are ignored, unless the D16752 has been selected by holding CSA/CSB low.

Baud Generator – The D16752 contains a programmable 16 bit baud generator that divides clock input by a divisor in the range, between 1 and (2^{16}–1). The output frequency of the baud generator is 16 × the baud rate. Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16752, in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM, to prevent long counts on initial load.

Modem Control Logic controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).

Interrupt Controller – D16752 contains fully prioritized interrupt system controller. It controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Identification (IIR) registers.

Receiver Control – Receiving starts, when the falling edge on Serial Input (RX) during IDLE State is detected. After starting, the R X input is sampled every 16 internal baud cycles, as it is shown in figure above. When the logic 1 state is detected during START bit, it means that the False Start bit was detected and receiver is back to the IDLE state.

Receiver FIFO – The R x FIFO can be 64 (128, 256, 512) levels deep, it receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time, if R x interrupts are enabled, the UART will issue an interrupt to the CPU. The R x FIFO will continue to store bytes, until it is full and will not accept any more bytes. Any further data entering the R x shift register will set the Overrun Error flag.

Transmitter Control module controls transmission of written to THR (Transmitter Holding register) character via serial output T X. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.

Transmitter FIFO – the T x portion of the UART transmits data through T X, as soon as the CPU loads a byte into the T x FIFO. The UART will prevent loads to the Tx FIFO, if it currently holds 64 (128, 256, 512) characters (depending on FCR (5) bit value and selected FIFO size). Loading to the T x FIFO will be enabled again, as soon, as the next character is transferred to the T x shift register. These capabilities account for the largely autonomous operation of the T x. The UART starts the above operations typically with a T x interrupt.

CONFIGURATION

The following parameters of the D16752 core can be easily adjusted to requirements of dedicated application and technology. Core configuration can be effortlessly done by changing appropriate constants in package file. There is no need to change any parts of the code.

- Baud generator: *enable / disable*
- External BAUDCLK source: *enable / disable*
- Channel B: *enable / disable*
- Modem Control: *enable / disable*
- SCR register: *enable / disable*
- FIFO Control logic: *enable / disable*
- FIFO Size: *normal 64 / large, up to 512*

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **XILINX®** devices after Place & Route:

Device	Speed grade	Slices	F_{max}
VIRTEX-IV	-11	864+4RAMs	125 MHz
VIRTEX-IIP	-7	854+4RAMs	125 MHz
VIRTEX-II	-6	854+4RAMs	100 MHz
VIRTEX-E	-8	856+4RAMs	72 MHz
VIRTEX	-6	856+4RAMs	56 MHz
SPARTAN-IIIE	-5	867+4RAMs	70 MHz
SPARTAN-III	-5	854+4RAMs	83 MHz
SPARTAN-IIE	-7	856+4RAMs	69 MHz
SPARTAN-II	-6	856+4RAMs	69 MHz

[1]– FIFOs implemented in RAM's – 2432 Bits

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

LICENSING

Transparent and clearly defined licensing methods without royalty-per-chip fees, make use of our IP Cores easy & simple.
– ***Single-Site license option*** – dedicated to small and middle sized companies, which run their business in one place.
– ***Multi-Site license option*** – dedicated to corporate customers who operate at several locations. The licensed product can be used in selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.
There are two formats of the delivered IP Core:
– VHDL or Verilog RTL synthesizable HDL Source code
– FPGA EDIF/NGO/NGD/QXP/VQM Netlist

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