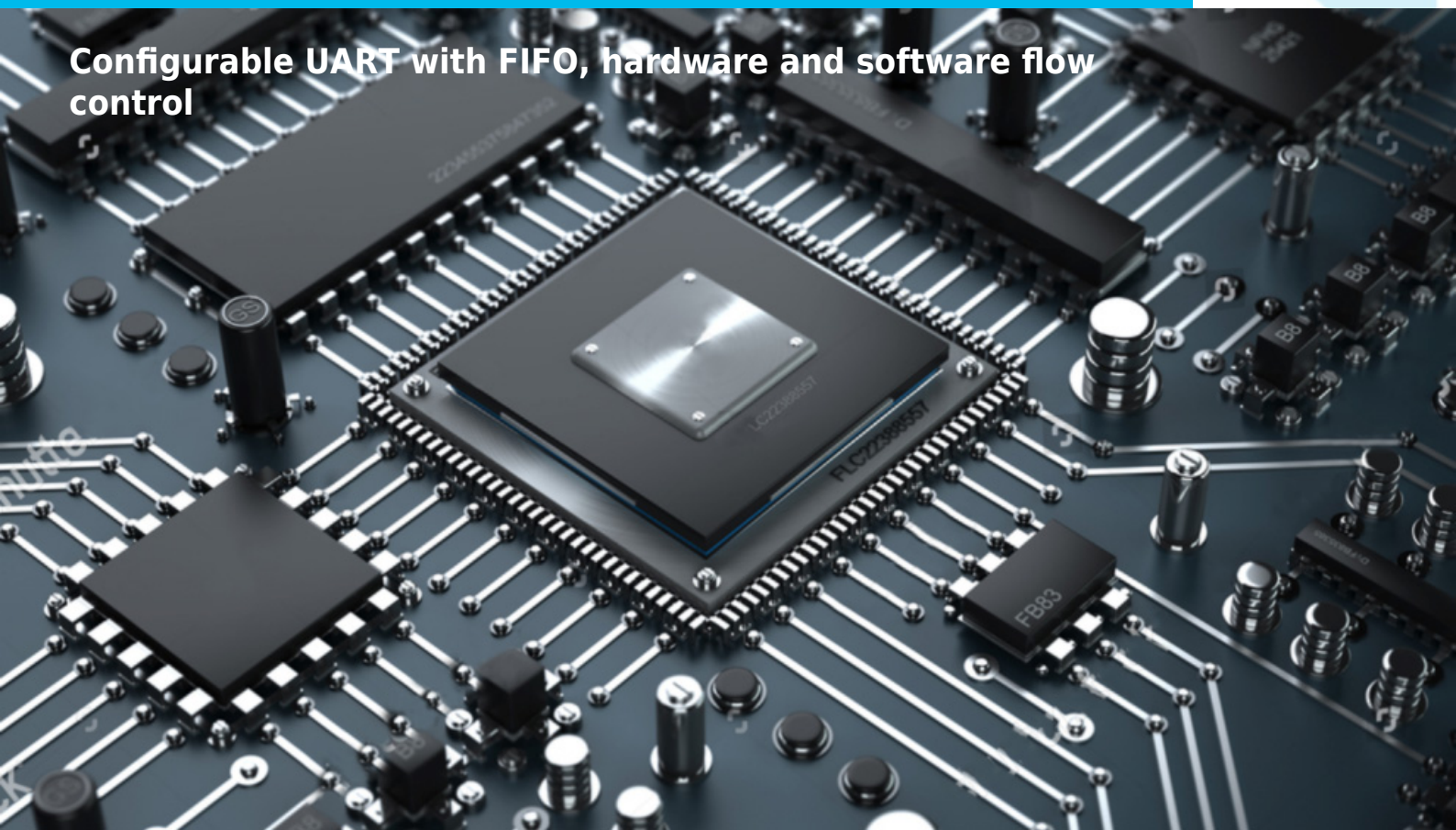
DIGITAL CORE DESIGN

D16752

Configurable UART with FIFO, hardware and software flow control



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D16752 UART IP Core – TL16C752-Compatible Dual-Channel UART

The **D16752 UART IP Core** from **DCD-SEMI** is a **highly configurable Universal Asynchronous Receiver/Transmitter (UART)** designed for **FPGA and ASIC integration**. Delivered as a **bridge to APB, AHB, and AXI bus architectures**, it is **software compatible with the TL16C752**, making it ideal for **legacy UART replacement**, **dual-channel communication**, and **embedded high-efficiency designs**.

Dual-Channel Operation with 64-Byte FIFOs

The D16752 supports **dual-channel UART operation** with **64-byte receive and transmit FIFOs per channel**, including **3 bits of error status per byte in the receiver FIFO**.

- Programmable **FIFO trigger levels**
- **FIFO RDY register** provides TXRDY/RXRDY status for all UART ports in a single access
- Alternate **FIFO mode** reduces CPU overhead and enables efficient DMA transfers

These features make it a perfect solution for **high-performance, low-latency serial communication**.

Enhanced Hardware and Software Flow Control

The D16752 includes **selectable hardware flow control** (RTS/CTS) and **software flow control** (programmable Xon/Xoff characters).

- **Hardware flow control** automatically regulates serial data flow, significantly reducing CPU load
- **Software flow control** ensures smooth communication in complex multi-UART systems
- **Transmission Control Register (TCR)** manages FIFO threshold levels to start/stop transmission efficiently

Complete Status Reporting and Error Detection

The core provides **full status visibility** for each channel, including:

- FIFO conditions and trigger status
- **Parity, framing, break, idle, and overflow errors**
- Modem interface operational status

This ensures **deterministic communication** and simplifies firmware integration.

Programmable Baud Rate and Flexible Clocking

The D16752 features a **programmable baud rate generator**, capable of dividing a reference clock by **1 to ($2^{16} - 1$)**, and generating a precise **16× clock for transmitter and receiver logic**.

- Separate **BAUD CLK input** allows exact transmission speed
- UART logic operates at CPU clock frequency
- Supports **5, 6, 7, or 8-bit characters**, even/odd/no parity, and 1, 1.5, or 2 stop bits

Configurable Architecture for Area Optimization

During synthesis, designers can:

- Enable/disable **Modem Control Logic**
- Enable/disable **FIFO Control Logic**
- Adjust **FIFO size**

Disabling unused features in area-constrained designs can **save up to 50% of logic resources**, making it compatible with **16450 mode operation**.

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Ideal for SoC and Standalone Designs

The D16752 is suitable for:

- **Shared clock domains** inside FPGA or ASIC
- **Standalone multi-UART implementations** with several UARTs in one chip

Its **universal CPU interface** simplifies implementation and verification by **reducing clock tree complexity**.

Verification-Ready and Technology Independent

Like all DCD-SEMI UART IP Cores, the D16752 includes a **fully automated testbench** and a **complete set of validation tests**, ensuring smooth SoC integration.

It is **technology-independent** and can be implemented across a wide range of **FPGA and ASIC process technologies**.

Typical Applications

- TL16C752 / dual-channel UART replacement
- High-performance embedded SoCs
- Industrial automation and instrumentation
- Multi-UART FPGA designs
- Communication-intensive applications requiring flow control

UART IP Core Family Comparison

The table below compares DCD-SEMI UART and serial communication IP Cores to help FPGA and ASIC design engineers quickly select the optimal solution for their project requirements.

Feature / IP Core	D16450	D16550	D16750	D16752	D16950	D8530	DMESCC
Primary Function	Classic UART	FIFO-based UART	High-performance UART	Dual-channel high-performance UART	High-throughput UART	Dual-channel USART	Dual-channel multiprotocol serial controller
UART Compatibility	16450 / TL16C450	16550 / TL16C550A	16750 / TL16C750	16752 / TL16C752	16450-16750 + OX16C950	Zilog 8530–compatible	Enhanced ESCC-compatible
Channels	1	1	1	2	1	2	2
Supported Modes	Asynchronous	Asynchronous & FIFO	Asynchronous & FIFO	Asynchronous & FIFO, dual-channel	Asynchronous & synchronous	Asynchronous & synchronous	Asynchronous & synchronous
FIFO Support	□ No FIFO	□ 16-byte FIFO	□ 512-byte FIFO	□ 64-byte FIFO per channel	□ 128-byte FIFO	Optional / limited	Optional / configurable
FIFO Trigger Levels	—	Configurable	Programmable (1–512)	Programmable per channel	Programmable (1–127)	—	—
CPU Load	High	Medium	Low	Low	Low	Medium	Medium
Error Reporting	Parity, framing, overrun, break	Parity, framing, overrun, break	Parity, framing, overrun, break	Parity, framing, overrun, break, idle	Parity, framing, overrun, break	Parity, CRC, abort	Parity, CRC, abort
CRC Generation / Check	No	No	No	No	No	Yes (sync modes)	Yes (sync modes)
Modem Control	Full	Full	Advanced autoflow	Hardware/software flow control, TCR	Advanced autoflow	Yes (both channels)	Yes (both channels)
Interrupt System	Programmable	Programmable	Advanced programmable	Programmable, FIFO RDY register	Advanced programmable	Programmable	Programmable
DMA Support	Interrupt-optimized	Interrupt-optimized	Yes	Yes	Yes	Yes	Yes
Clocking Options	Internal BRG	Internal BRG	Internal / external	Internal / external	Internal / external	Internal BRG	Internal BRG
Special Features	Legacy compatibility	Configurable FIFO & Modem	Deep FIFO (512B), autoflow, 16450 modes	Dual-channel, FIFO RDY register, hardware/software flow control, TCR	Deep FIFO, 9-bit mode, synchronous	Legacy protocol support (HDLC, SDLC)	Enhanced block transfer, vectored interrupts
Typical Applications	Legacy UART replacement	FIFO-based legacy upgrade	High-throughput UART, legacy replacement	Dual-channel embedded UART, TL16C752 replacement	Telecom, industrial gateways	Telecom, LAN, industrial serial	Communications controllers, protocol engines
Bus Interfaces	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI
Technology Independence	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Selection Guidelines

- **Choose D16450** for exact legacy 16450 / TL16C450 replacement.
- **Choose D16550** when FIFO buffering and moderate CPU optimization are required.
- **Choose D16750** for high-performance legacy replacement with deep FIFO and low CPU load.
- **Choose D16752** for **dual-channel high-performance UART** with hardware/software flow control and 64-byte FIFOs.
- **Choose D16950** for high-throughput UART with deep FIFO, synchronous mode, and advanced flow control.
- **Choose D8530** when dual-channel USART and legacy protocol support are required.
- **Choose DMESCC** for advanced multiprotocol serial communication and block handling.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Software compatible with 16752 UARTs
- **Configuration capability**
- **Dual channel UART – configurable**
- **Separate configurable BAUD clock line**
- **Supports RS232 and RS485 standards**
- **Hardware/Software Data flow control**
  - Programmable Xon/Xoff characters
  - Programmable AutoRTS, AutoCTS
- **Programmable and selectable Transmit and Receive FIFO Trigger levels for DMA and interrupt generation**
- **Programmable Receive FIFO Trigger Levels for Software/Hardware Flow Control**
- **Software Flow Control Turned OFF, optionally by any Xon Rx Character**
- Software Selectable Baud Rate Generator Prescaleable Clock Rates of 1x and 4x
- **Programmable SLEEP Mode**
- Majority Voting Logic
- Two modes of operation: UART mode and FIFO mode
  - In the FIFO mode transmitter and receiver are each buffered with 64 byte FIFO to reduce the number of interrupts presented to the CPU
  - In UART mode receiver and transmitter are double buffered to eliminate a need for precise

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synchronization between the CPU and serial data
- Configurable **FIFO size** allowing **up to 512 levels** deep FIFOs in both Rx and Tx directions.
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial interface characteristics:
  - 5-, 6-, 7- or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1.5-, or 2-stop bit generation
  - Internal baud generator
- **Complete status reporting capabilities**
- Line break generation and detection. Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- Fully synthesizable
- Static synchronous design and no internal tri-states

OPTIONAL FEATURES

- IEEE 1284 Bidirectional Parallel Data Port
  - *Compatible with Standard Centronics Parallel Interface*
  - *Support for Parallel Protocols: ECP and EPP*
  - *Data Path 16/64-Byte FIFO Buffer*
  - *Direct Memory Access (DMA) Transfer*
  - *Decompression of Run Length Encoded Data in ECP Reserve Mode*
  - *Direct Connection to Printer, No External Transceiver is needed*
- Serial Ports with Infrared Data Association (IRDA) inputs and outputs

DESIGN FEATURES

The functionality of the D16752 core was based on the Texas Instruments' TL16C752. The following characteristics differentiate the D16752 from Texas Instruments' devices:

- The bi-directional data bus has been split into two separate buses: datai (7:0), datao (7:0)
- The DLL, DLM and THR registers are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge following a THR write
- Asynchronous microcontroller interface is replaced by equivalent Universal interface
- All latches implemented in original 16752 devices are replaced by equivalent flip-flop registers, with the same functionality

UNITS SUMMARY

Data Bus Buffer – The data Bus Buffer accepts inputs from the system bus and generates control signals for other D16752 functional blocks. Address bus ADDR (2:0) selects one of the register to be read from/written into. Both, RD and WE signals, are active low and are qualified by CSA / CSB; RD and WE are ignored, unless the D16752 has been selected by holding CSA/CSB low.

Baud Generator – The D16752 contains a programmable 16 bit baud generator that divides clock input by a divisor in the range, between 1 and (2^{16}–1). The output frequency of the baud generator is 16 × the baud rate. Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16752, in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM, to prevent long counts on initial load.

Modem Control Logic controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).

Interrupt Controller – D16752 contains fully prioritized interrupt system controller. It controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Identification (IIR) registers.

Receiver Control – Receiving starts, when the falling edge on Serial Input (RX) during IDLE State is detected. After starting, the R X input is sampled every 16 internal baud cycles, as it is shown in figure above. When the logic 1 state is detected during START bit, it means that the False Start bit was detected and receiver is back to the IDLE state.

Receiver FIFO – The R x FIFO can be 64 (128, 256, 512) levels deep, it receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time, if R x interrupts are enabled, the UART will issue an interrupt to the CPU. The R x FIFO will continue to store bytes, until it is full and will not accept any more bytes. Any further data entering the R x shift register will set the Overrun Error flag.

Transmitter Control module controls transmission of written to THR (Transmitter Holding register) character via serial output T X. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.

Transmitter FIFO – the T x portion of the UART transmits data through T X, as soon as the CPU loads a byte into the T x FIFO. The UART will prevent loads to the Tx FIFO, if it currently holds 64 (128, 256, 512) characters (depending on FCR (5) bit value and selected FIFO size). Loading to the T x FIFO will be enabled again, as soon, as the next character is transferred to the T x shift register. These capabilities account for the largely autonomous operation of the T x. The UART starts the above operations typically with a T x interrupt.

CONFIGURATION

The following parameters of the D16752 core can be easily adjusted to requirements of dedicated application and technology. Core configuration can be effortlessly done by changing appropriate constants in package file. There is no

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need to change any parts of the code.

- Baud generator: *enable / disable*
- External BAUDCLK source: *enable / disable*
- Channel B: *enable / disable*
- Modem Control: *enable / disable*
- SCR register: *enable / disable*
- FIFO Control logic: *enable / disable*
- FIFO Size: *normal 64 / large, up to 512*

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **AMD FPGA** devices after Place & Route:

Device	Speed grade	Slices	F_{max}
VIRTEX-IV	-11	864+4RAMs	125 MHz
VIRTEX-IIP	-7	854+4RAMs	125 MHz
VIRTEX-II	-6	854+4RAMs	100 MHz
VIRTEX-E	-8	856+4RAMs	72 MHz
VIRTEX	-6	856+4RAMs	56 MHz
SPARTAN-IIIE	-5	867+4RAMs	70 MHz
SPARTAN-III	-5	854+4RAMs	83 MHz
SPARTAN-IIE	-7	856+4RAMs	69 MHz
SPARTAN-II	-6	856+4RAMs	69 MHz

[1]– FIFOs implemented in RAM's – 2432 Bits

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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