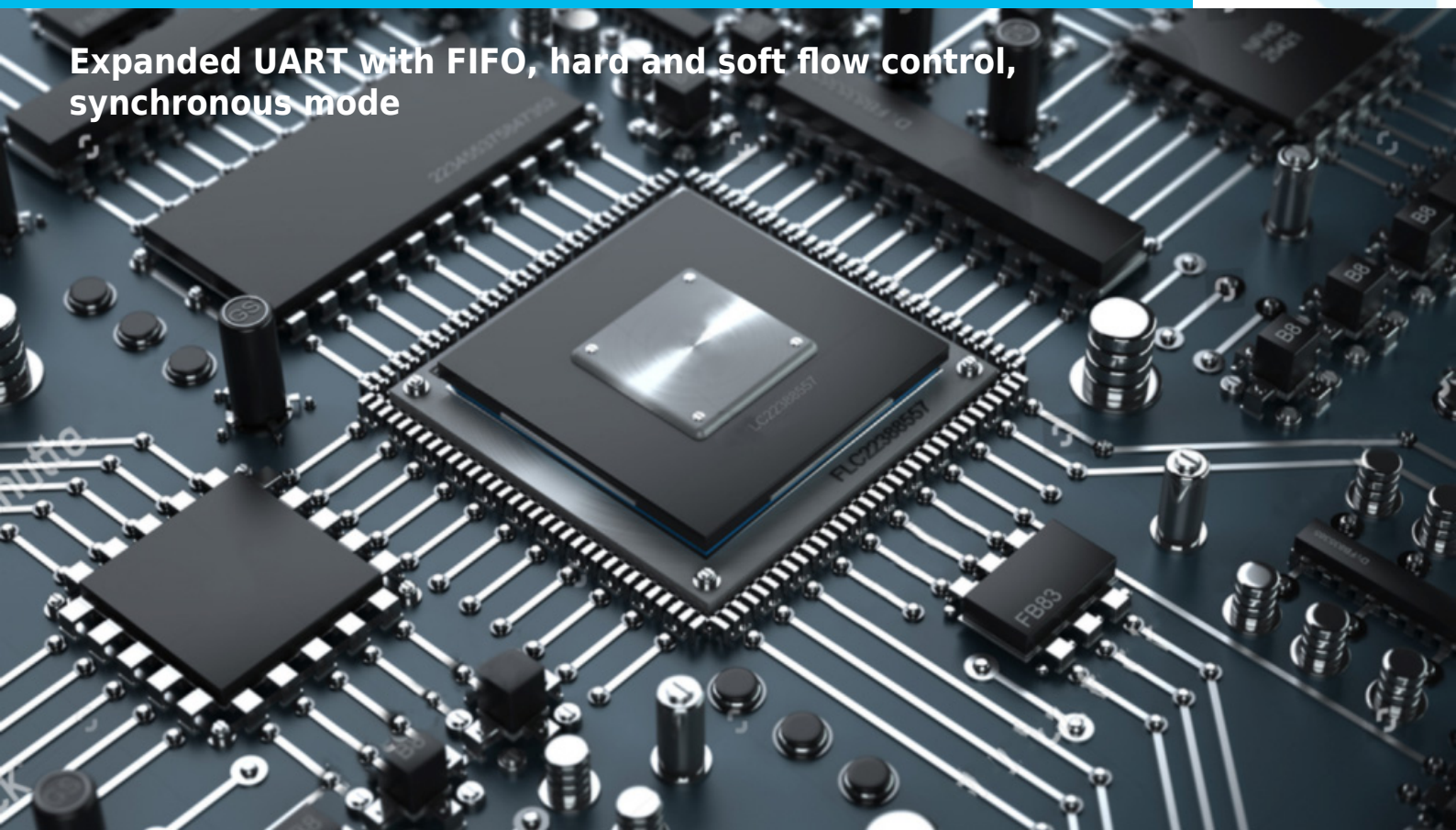
DIGITAL CORE DESIGN

D16950

Expanded UART with FIFO, hard and soft flow control, synchronous mode



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D16950 bridge to APB, AHB, AXI bus, it is a soft core of a Universal Synchronous and Asynchronous Receiver/Transmitter (UART), functionally compatible to the OX16C950. It allows **serial transmission in two modes: UART and FIFO**. In the FIFO mode, internal FIFOs are activated allowing 128 bytes (plus 3 bits of error data per byte in the RCVR FIFO) to be stored in both receive and transmit modes. Our efficient Core performs serial-to-parallel conversion on data characters received from a peripheral device or MODEM, but also parallel-to-serial conversion on data characters received from the CPU. The processor can read the complete status of the UART at **any time during the functional operation**. The reported status information includes the type and condition of transfer operations performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt). The **D16950 includes a programmable baud rate generator** which is able to divide a timing reference clock input by divisors of 1 to (216-1) and produce an n × clock for driving internal transmitter logic. Provisions are also included to use this n × clock to drive receiver logic. We also equipped our core with **complete MODEM-control capability** and a processor-interrupt system. Interrupts can be programmed according to your requirements, minimizing the computing required to handle the communications link. **The D16950 core includes all (16450, 16550, 16650 and 16750) features and additional functions**. The D16950 has ICR registers which give additional capabilities of UART work configuration. Data transmission may be synchronized by an external clock connected to the RI (for receiver and transmitter) or DSR (only for receiver) pin. The NMR register allows 9-bit mode transmission with or without special character. Writing and reading from/to FIFO may be controlled by trigger level registers. Trigger level registers may be set any value from 1 to 127. In the FIFO mode, there is a **selectable autoflow control feature** that can reduce software overload significantly and automatically increase system efficiency by controlling serial data flow through the **RTS output** and **CTS input** signals. The Core is perfect for applications **where** the **UART core and microcontroller are clocked by the same clock signal and are implemented inside the same ASIC or FPGA chip**. Nevertheless, it's also a proprietary solution for standalone implementation, where several UARTs are required to be implemented inside a single chip and driven by some off-chip devices. Thanks to a universal interface, **D16950 core implementation and verification are very simple**, just by eliminating a number of clock trees in the complete system. Like all our UART Cores, the D16950 includes a **fully automated test bench** with a **complete set of tests**, allowing easy package validation at each stage of the SoC design flow. This efficient solution is a technology-independent design that can be implemented in a variety of process technologies.

Watch the D16950 presentation on DCD's YouTube:

As Seen On YouTube

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FATURES

- Software compatible with 16450, 16550,16650,16750 and 16950 UARTs
- Synchronous and Asynchronous transmission
- **Configuration capability**
- Supports RS232 and RS485 standards
- Separate configurable BAUD clock line
- Supports IRDA data format mode
- Majority Voting Logic
- Two modes of operation: UART mode and FIFO mode
  - In the FIFO mode transmitter and receiver are each buffered with 128 byte FIFO to reduce the number of interrupts presented to the CPU
  - In UART mode receiver and transmitter are double buffered to eliminate a need for precise synchronization between the CPU and serial data
- FIFO size – 128 Bytes
- Optional FIFO size extension to 256 or 512 Bytes
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI, DCD)
- Programmable Hardware Flow Control through RTS and CTS
- Programmable Flow Control using DTR and DSR

- Programmable in-band Flow Control using XON/XOFF
- Programmable special characters detection
- Trigger levels for TX and RX FIFO
- Interrupts and automatic in-band and out-off-band flow control
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, 8- or 9-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1.5-, or 2-stop bit generation
  - Internal baud generator
  - Detection of bad data in receiver FIFO
- Clock prescaler from 1 to 31,875
- Enhanced isochronous clock option
- 9- bit data mode
- Software reset
- Complete status reporting capabilities
- Line break generation and detection. Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**
- Fully synthesizable
- Static synchronous design and no internal tri-states

UNITS SUMMARY

Data Bus Buffer – The data Bus Buffer accepts inputs from the system bus and generates control signals for other D16950 functional blocks. Address bus ADDR (2:0) selects one of the register to be read from/written into. Both RD and WE signals are active low and are qualified by CS; RD and WE are ignored, unless the D16950 has been selected by holding CS low.

Baud Generator – The D16950 contains a programmable 16 bit baud generator that divides clock input by a divisor, in the range between 1 and (2^{16}–1). Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16950, in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM, to prevent long counts on initial load. In addition, prescaler register is provided, which can further divide the clock by values in the range 1,0 to 31,875 in steps of 0,125. Other additional option is the Time Clock Register (TCR), which allows set the sampling clock between 4 and 16 values.

Modem Control Logic controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).

Interrupt Controller – D16950 contains fully prioritized interrupt system controller. It is enabled by INTSEL pin. It controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Status (ISR) registers.

Receiver Control – Receiving starts, when the falling edge on Serial Input (SI) during IDLE State is detected. After starting the SI input is sampled every 16 internal baud cycles, as it is shown in figure on the previous page. When the logic 1 state is detected during START bit, it means, that the False Start bit was detected and receiver is back to the IDLE state.

Receiver FIFO – The R x FIFO is 128 levels deep, it receives data, until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time, if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes, until it is full and will not accept any more bytes. Any further data entering the R x shift register, will set the Overrun Error flag.

Transmitter Control – Controls transmission of written to THR (Transmitter Holding register) character via serial output SO. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.

Transmitter FIFO – the T x portion of the UART transmits data through SO, as soon as the CPU loads a byte into the T x FIFO. The UART will prevent loads to the Tx FIFO; if it currently holds 128 characters (depending on FCR (5) bit value and selected FIFO size). Loading to the T x FIFO will be enabled again, as soon as the next character is transferred to the T x shift register. These capabilities account for the largely autonomous operation of the T x. The UART starts the above operations typically with a T x interrupt.

DESIGN FEATURES

The functionality of the D16950 core is based on the Oxford Semiconductor's OX16C950. The following characteristics differentiate the D16950 from Oxford Semiconductor's devices:

- The bidirectional data bus has been split into two separate buses: datai (7:0), datao (7:0)
- The DLL, DLM and THR register are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge following a THR write
- Fully synthesizable static design with no internal tri-state buffers
- All latches implemented in original 16950 devices are replaced by equivalent flip-flop registers, with the same functionality

CONFIGURATION

The following parameters of the D16950 core can be easily adjusted to requirements of proprietary application and technology. Core configuration can be effortlessly done by changing appropriate constants in package file. There is no need to change any part of the code.

- FIFO Size: *normal 16/128 / large, up to 512*

APPLICATIONS

- Serial Data communications applications

- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC®** devices:

Technology	Optimization	Gates	F_{max}
0.25 typical	area	11 000	150 MHz
0.25 typical	speed	12 500	300 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
  - Delivery of the IP Core and documentation updates
  - Phone & email support
  - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)
HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

Digital Core Design Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/