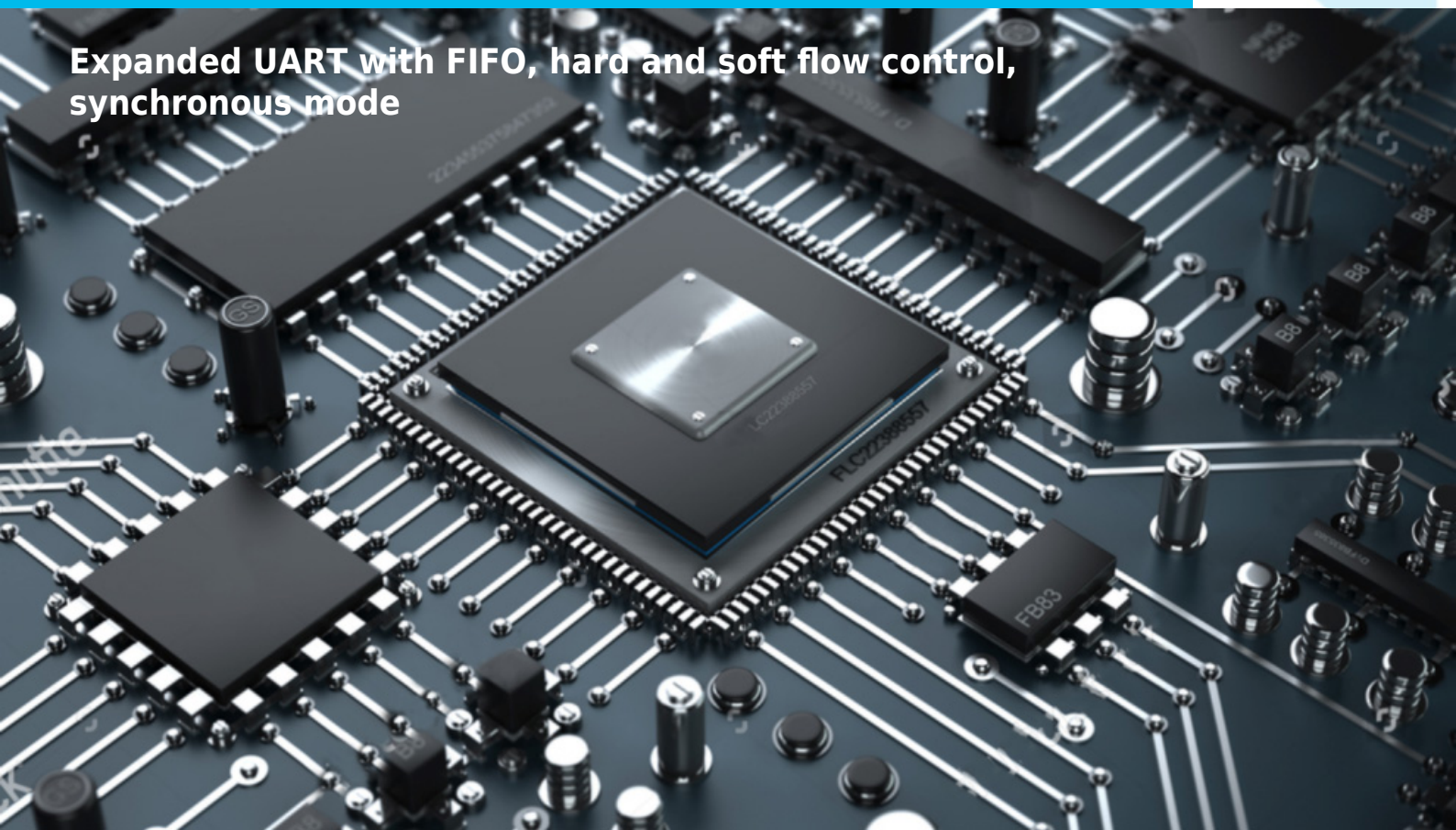
DIGITAL CORE DESIGN

D16950

Expanded UART with FIFO, hard and soft flow control, synchronous mode



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D16950 UART IP Core – High-Performance UART with 128-Byte FIFO for FPGA & ASIC

The **D16950 UART IP Core** from **DCD-SEMI** is a high-performance **Universal Synchronous/Asynchronous Receiver/Transmitter (UART)** designed for **FPGA and ASIC integration**. Delivered as a scalable **bridge to APB, AHB, and AXI bus architectures**, the D16950 is **functionally compatible with the OX16C950** and fully backward compatible with **16450, 16550, 16650, and 16750 UART standards**, while offering extended configuration and performance features.

The core supports serial communication in both **standard UART mode** and **high-throughput FIFO mode**, making it suitable for demanding embedded and SoC applications.

Deep FIFO Architecture for High Throughput

In FIFO mode, the D16950 activates internal FIFOs allowing:

- **128-byte transmit FIFO**
- **128-byte receive FIFO**, with an additional **3 bits of error status per received byte**

This architecture significantly reduces interrupt frequency and CPU load while enabling reliable high-speed serial communication.

Comprehensive Status Reporting and Error Handling

The processor can read the **complete UART status at any time** during operation. Reported status information includes:

- Transfer operation state
- Parity, overrun, framing, and break errors
- FIFO conditions and interrupt sources

This ensures robust diagnostics and predictable system behavior.

Programmable Baud Rate and Clocking Flexibility

The D16950 includes a **programmable baud rate generator** capable of dividing a reference clock by divisors from **1 to ($2^{16} - 1$)** to generate an **n× clock** for internal transmitter logic. The same clock can also drive receiver logic.

Additionally, data transmission can be **synchronized to an external clock**, connected via:

- **RI pin** (receiver and transmitter)
- **DSR pin** (receiver only)

This flexibility makes the core suitable for both synchronous and asynchronous applications.

Advanced UART Features and Flow Control

Key advanced capabilities include:

- Full **MODEM control** (RTS, CTS, DTR, DSR, DCD, RI)
- **Programmable interrupt system** to minimize CPU overhead
- **Trigger-level control** for FIFO read/write operations (1–127 bytes)
- **Selectable autoflow control**, automatically managing RTS/CTS signals
- **9-bit mode transmission** via NMR register, with or without special character support

The **ICR registers** provide additional UART configuration options beyond legacy devices.

Optimized for SoC Integration and Multi-UART Designs

The D16950 is ideal for systems where the **UART core and microcontroller share the same clock domain** inside a single FPGA or ASIC. Its **universal interface** simplifies implementation and verification by eliminating unnecessary clock domain crossings.

The core is also well suited for **standalone multi-UART designs**, where multiple UART instances are implemented within one chip and driven by off-chip devices.

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Verification-Ready and Technology Independent

Like all DCD-SEMI UART solutions, the D16950 includes a **fully automated testbench with a comprehensive test suite**, enabling straightforward validation throughout the entire SoC design flow.

The IP Core is **technology-independent** and can be implemented across a wide range of **FPGA and ASIC process technologies**.

Typical Applications

- FPGA and ASIC SoCs
- Multi-UART communication controllers
- Industrial and telecom systems
- Embedded controllers with high serial bandwidth requirements
- Legacy UART replacement with enhanced performance

Watch the D16950 presentation on DCD's YouTube:



UART IP Core Family Comparison

The table below compares DCD-SEMI UART and serial communication IP Cores to help FPGA and ASIC design engineers quickly select the optimal solution for their project requirements.

Feature / IP Core	D16950	D8530	DMESCC
Primary Function	High-performance UART	Dual-channel USART	Dual-channel multiprotocol serial controller
UART Compatibility	16450 / 16550 / 16650 / 16750 / OX16C950	Zilog 8530–compatible	Enhanced ESCC-compatible
Channels	1	2	2
Supported Modes	Asynchronous & synchronous	Asynchronous & synchronous	Asynchronous & synchronous
FIFO Support	Yes – 128 TX / 128 RX	Optional / limited	Optional / configurable
Error Reporting	Parity, framing, overrun, break	Parity, CRC, abort	Parity, CRC, abort
CRC Generation / Check	No	Yes (sync modes)	Yes (sync modes)
Modem Control	Full (RTS, CTS, DTR, DSR, DCD, RI)	Yes (both channels)	Yes (both channels)
Interrupt System	Fully programmable	Programmable	Programmable
DMA Support	Interrupt-optimized (DMA-friendly)	Yes	Yes
Clocking Options	Internal BRG, external sync clock	Internal BRG	Internal BRG
Special Features	Autoflow control, 9-bit mode, deep FIFO	Legacy protocol support (HDLC, SDLC)	Enhanced block transfer, vectored interrupts
Typical Applications	High-throughput UART, legacy UART replacement	Telecom, LAN, industrial serial	Communications controllers, protocol engines
Bus Interfaces	APB, AHB, AXI	APB, AHB, AXI	APB, AHB, AXI
Technology Independence	Yes	Yes	Yes

Selection Guidelines

- **Choose D16950** for high-bandwidth UART communication with minimal CPU load and legacy UART compatibility.
- **Choose D8530** when classic dual-channel USART functionality and protocol flexibility are required.
- **Choose DMESCC** for advanced multiprotocol serial communication with enhanced control and block handling.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FATURES

- Software compatible with 16450, 16550,16650,16750 and 16950 UARTs
- Synchronous and Asynchronous transmission
- **Configuration capability**
- Supports RS232 and RS485 standards
- Separate configurable BAUD clock line
- Supports IRDA data format mode
- Majority Voting Logic
- Two modes of operation: UART mode and FIFO mode
  - In the FIFO mode transmitter and receiver are each buffered with 128 byte FIFO to reduce the number of interrupts presented to the CPU
  - In UART mode receiver and transmitter are double buffered to eliminate a need for precise synchronization between the CPU and serial data
- FIFO size – 128 Bytes
- Optional FIFO size extension to 256 or 512 Bytes
- Adds or deletes standard asynchronous communication bits (start, stop and parity) to or from the serial data
- Independently controlled transmit, receive, line status and data set interrupts
- False start bit detection
- 16 bit programmable baud generator
- Independent receiver clock input
- MODEM control functions (CTS, RTS, DSR, DTR, RI, DCD)
- Programmable Hardware Flow Control through RTS and CTS
- Programmable Flow Control using DTR and DSR
- Programmable in-band Flow Control using XON/XOFF

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- Programmable special characters detection
- Trigger levels for TX and RX FIFO
- Interrupts and automatic in-band and out-off-band flow control
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, 8- or 9-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1.5-, or 2-stop bit generation
  - Internal baud generator
  - Detection of bad data in receiver FIFO
- Clock prescaler from 1 to 31,875
- Enhanced isochronous clock option
- 9- bit data mode
- Software reset
- Complete status reporting capabilities
- Line break generation and detection. Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- Fully synthesizable
- Static synchronous design and no internal tri-states

UNITS SUMMARY

Data Bus Buffer – The data Bus Buffer accepts inputs from the system bus and generates control signals for other D16950 functional blocks. Address bus ADDR (2:0) selects one of the register to be read from/written into. Both RD and WE signals are active low and are qualified by CS; RD and WE are ignored, unless the D16950 has been selected by holding CS low.

Baud Generator – The D16950 contains a programmable 16 bit baud generator that divides clock input by a divisor, in the range between 1 and (2^{16}–1). Two 8-bit registers, called divisor latches DLL and DLM, store the divisor in a 16-bit binary format. These divisor latches must be loaded during initialization of the D16950, in order to ensure desired operation of the baud generator. When either of the divisor latches is loaded, a 16-bit baud counter is also loaded on the CLK rising edge, following the write to DLL or DLM, to prevent long counts on initial load. In addition, prescaler register is provided, which can further divide the clock by values in the range 1,0 to 31,875 in steps of 0,125. Other additional option is the Time Clock Register (TCR), which allows set the sampling clock between 4 and 16 values.

Modem Control Logic controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM).

Interrupt Controller – D16950 contains fully prioritized interrupt system controller. It is enabled by INTSEL pin. It controls interrupt requests to the CPU and interrupt priority. Interrupt controller contains Interrupt Enable (IER) and Interrupt Status (ISR) registers.

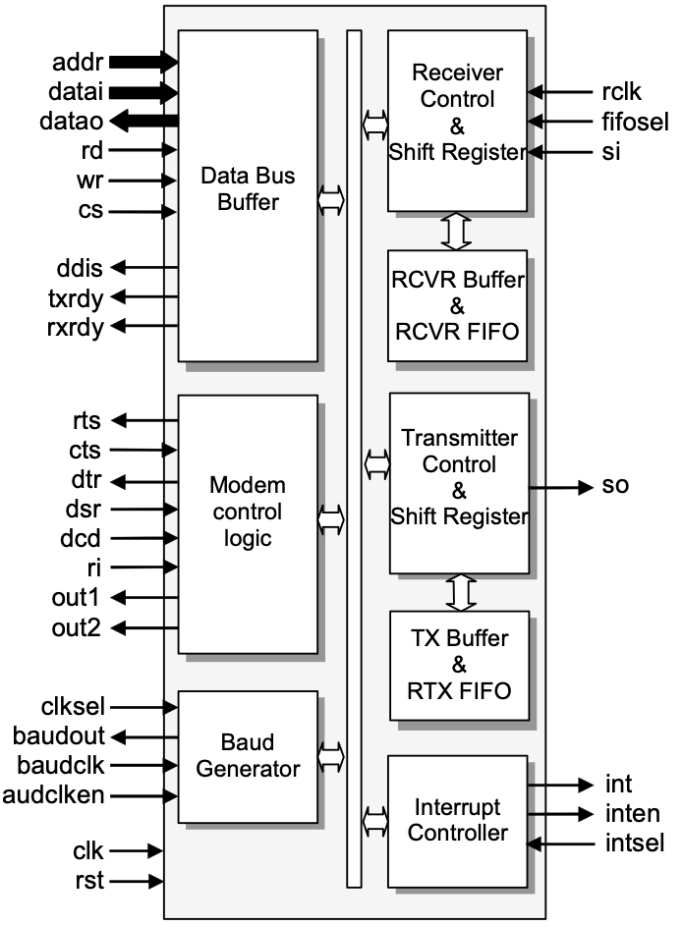
Receiver Control – Receiving starts, when the falling edge on Serial Input (SI) during IDLE State is detected. After starting the SI input is sampled every 16 internal baud cycles, as it is shown in figure on the previous page. When the logic 1 state is detected during START bit, it means, that the False Start bit was detected and receiver is back to the IDLE state.

Receiver FIFO – The R x FIFO is 128 levels deep, it receives data, until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time, if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes, until it is full and will not accept any more bytes. Any further data entering the R x shift register, will set the Overrun Error flag.

Transmitter Control – Controls transmission of written to THR (Transmitter Holding register) character via serial output SO. The new transmission starts on the next overflow signal of internal baud generator, after writing to THR register or Transmitter FIFO. Transmission control contains THR register and transmitter shift register.

Transmitter FIFO – the T x portion of the UART transmits data through SO, as soon as the CPU loads a byte into the T x FIFO. The UART will prevent loads to the Tx FIFO; if it currently holds 128 characters (depending on FCR (5) bit value and selected FIFO size). Loading to the T x FIFO will be enabled again, as soon as the next character is transferred to the T x shift register. These capabilities account for the largely autonomous operation of the T x. The UART starts the above operations typically with a T x interrupt.

BLOCK DIAGRAM



CONFIGURATION

The following parameters of the D16950 core can be easily adjusted to requirements of proprietary application and

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technology. Core configuration can be effortlessly done by changing appropriate constants in package file. There is no need to change any part of the code.

- FIFO Size: *normal 16/128 / large, up to 512*

DESIGN FEATURES

The functionality of the D16950 core is based on the Oxford Semiconductor's OX16C950. The following characteristics differentiate the D16950 from Oxford Semiconductor's devices:

- The bidirectional data bus has been split into two separate buses: datai (7:0), datao (7:0)
- The DLL, DLM and THR register are reset to all zeros
- TEMT and THRE bits of Line Status Register, are reset during the second clock rising edge following a THR write
- Fully synthesizable static design with no internal tri-state buffers
- All latches implemented in original 16950 devices are replaced by equivalent flip-flop registers, with the same functionality

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **AMD FPGA** devices, after Place & Route:

Device	LUTs/Slices	Memory Blocks	F_{max}
ZYNQ	667/344	2	183 MHz
ZYNQ 7000	598	1	330 MHz
KINTEX 7	675/349	2	322 MHz
KINTEX Ultra Scale	598	1	330 MHz
ARTIX 7	627/341	2	167 MHz
VIRTEX Ultra Scale	597	1	330 MHz
VIRTEX 7	681/359	2	318 MHz
VIRTEX 6	618/331	2	175 MHz
VIRTEX 5	740/342	2	244 MHz
VIRTEX 4	984/704	2	165 MHz
SPARTAN 6	619/260	2	137 MHz
SPARTAN 3E	975/694	2	107 MHz
SPARTAN 3	982/704	2	102 MHz

FIFOs implemented in RAM's – 2560 Bits

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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