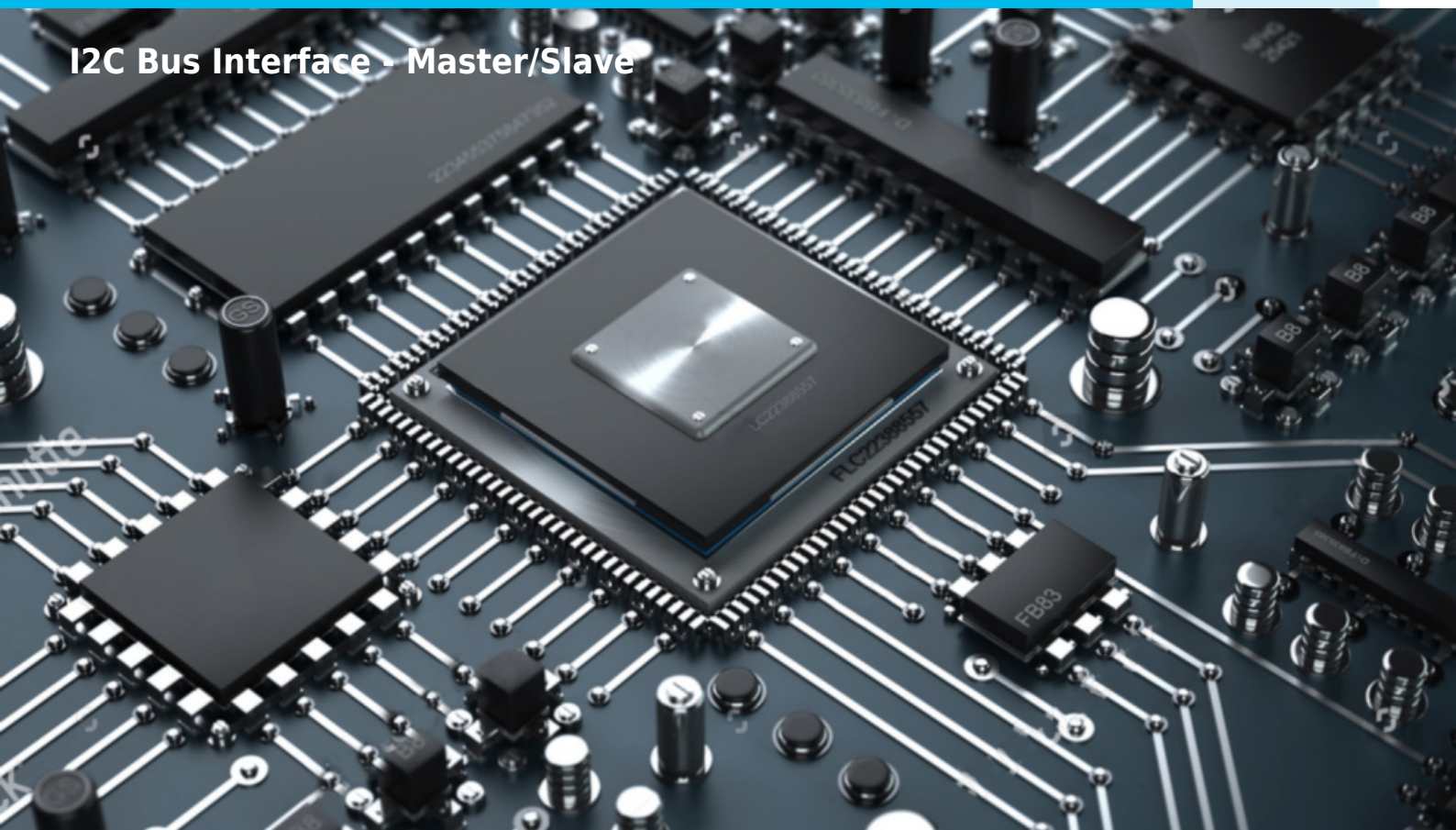
DIGITAL CORE DESIGN

DI2CMS

I2C Bus Interface - Master/Slave



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DI2CMS IP Core – I2C, SMBus & PMBus Controller for FPGA & ASIC

The **DI2CMS IP Core** from **DCD-SEMI** is a flexible and robust **I2C bus controller** designed to seamlessly bridge **microprocessors and SoC architectures** with **I2C, SMBus, and PMBus** interfaces. Fully compliant with the **I2C v3.0 specification**, DI2CMS enables reliable serial communication in modern **FPGA and ASIC designs**.

The core consists of two tightly integrated modules: **DI2CM (I2C Master)** and **DI2CS (I2C Slave)**, allowing the IP Core to operate as either a **master or slave device** on the bus. This dual-mode capability makes DI2CMS suitable for a wide range of embedded, industrial, and power-management applications.

Advanced I2C Features for Complex Systems

DI2CMS supports advanced I2C capabilities required in sophisticated multi-device environments, including:

- **Multi-master arbitration**
- **Clock synchronization**
- **Controller clock stretching**
- Full support for **SMBus and PMBus protocols**

These features ensure reliable operation in **multi-master systems** and enable seamless interoperability with a broad ecosystem of I2C-compatible devices.

Full-Speed I2C, SMBus and PMBus Operation

The DI2CMS IP Core supports **configurable transmission speeds up to 3.4 Mb/s**, covering all standard and extended I2C operating modes:

- **Normal mode** – 100 kHz
- **Fast mode** – 400 kHz
- **Fast-plus mode** – 1 MHz
- **High-Speed mode** – 3.4 MHz

In addition, the core supports **all predefined SMBus and PMBus clock frequencies**, making it ideal for **system monitoring, power management, and control applications**.

SoC-Friendly Integration and Scalability

Designed with technology independence in mind, DI2CMS integrates easily into a wide range of SoC architectures. Supported CPU interfaces include:

- **AMBA APB**
- **AMBA AHB**
- **AMBA AXI**

The IP Core is suitable for implementation across multiple **FPGA and ASIC process technologies** and can be fully customized to meet application-specific requirements, optimizing area, performance, and power consumption.

Verified and Production-Ready IP

To ensure smooth integration into the SoC design flow, the DI2CMS IP Core is delivered with:

- **Automated testbench**
- **Comprehensive verification test suite**
- Proven compliance with **I2C v3.0, SMBus, and PMBus standards**

This validation infrastructure accelerates design verification and reduces integration risk.

Typical Applications

- Power management and voltage regulation (PMBus)
- System monitoring and control (SMBus)

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- Embedded controllers and SoCs
- Industrial and automotive electronics
- FPGA-based platforms requiring I2C connectivity

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Conforms to the I2C v3.0 specification
- Support for SMBus and PMBus protocols
- Both master and slave transmitter/receiver modes
- Multi-master support with bus arbitration
- Controller clock stretching and synchronization
- Clock stretching warning signal
- Clock low timeout detection
- User-configurable clock and data timings via:
  - Sythesis parameters
  - Dynamic registers reconfiguration
- 7 and 10-bit addressing in master mode
- SMBus Alert and PMBus control line support
- Up to 8 target addresses in slave mode
- Dynamic ACK bit control based on received data
- FIFO support in slave mode
- DMA support
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

UNITS SUMMARY

CPU Interface – Performs the interface functions between DI2CMS internal blocks and microprocessor. Allows easy connection between the core and a microprocessor / microcontroller system.
Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.
Shift Register – Controls SDA line, performs data and address shifts during the data transmission and reception.
Control Register – Contains five control bits, used for performing all types of I^2C Bus transmissions.
Status Register – Contains seven status bits that indicate state of the I^2C Bus and the DI2CMS core.
Input Filter – Performs spike filtering.
Clock Control Logic – Performs clock synchronization, clock generation in master mode and clock stretching in slave mode.
Arbitration Logic – Performs arbitration during operations in multi-master systems.
Timer – Allows operation from a wide range of the input frequencies. It is programmed by the user before transmission and can be reprogrammed to change the SCL frequency.
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BLOCK DIAGRAM

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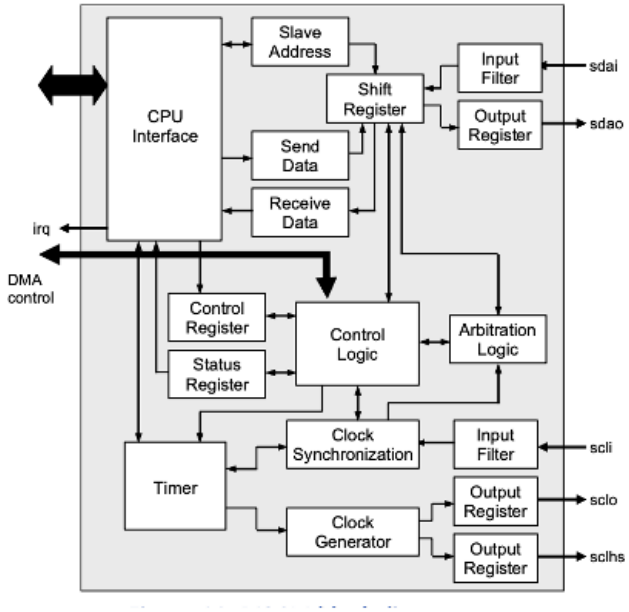
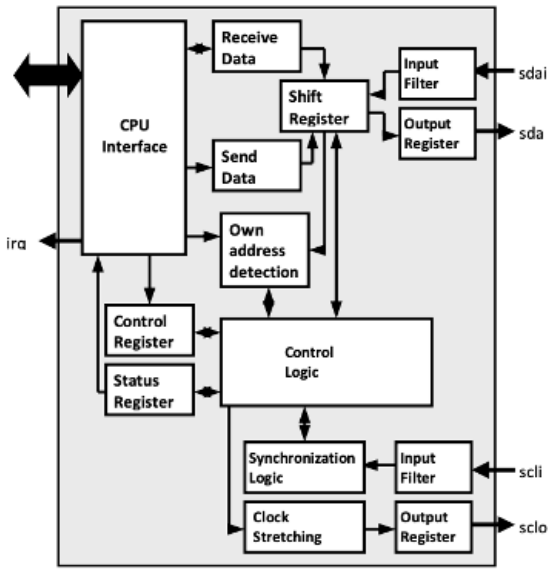


DI2CM Block Diagram



DI2CS Block Diagram

PERFORMANCE

The following table gives a survey about the Core area and performance in **AMD FPGA** devices after Place & Route (all key features included):

Family	Device	Speed grade	LUT	Slice	F_{max}
Spartan-3	xc3s50	-5	424	286	161 MHz
Spartan-3E	xc3s100e	-5	417	285	166 MHz
Spartan-6	xc6slx4	-3	289	119	269 MHz
Virtex-4	xc4vfx12	-12	464	290	310 MHz
Virtex-5	xc5vlx20t	-2	313	173	382 MHz
Virtex-6	xc6vlx75t	-3	290	93	375 MHz
Virtex-7	xc7vx330t	-3	324	109	492 MHz
Kintex-7	xc7k70t	-3	321	129	511 MHz
Artix-7	xc7a100t	-3	292	119	329 MHz
Virtex UltraScale	xcvu065	-3	376	57	500 MHz
Zynq-7000	xc7z010	-3	374	112	330 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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