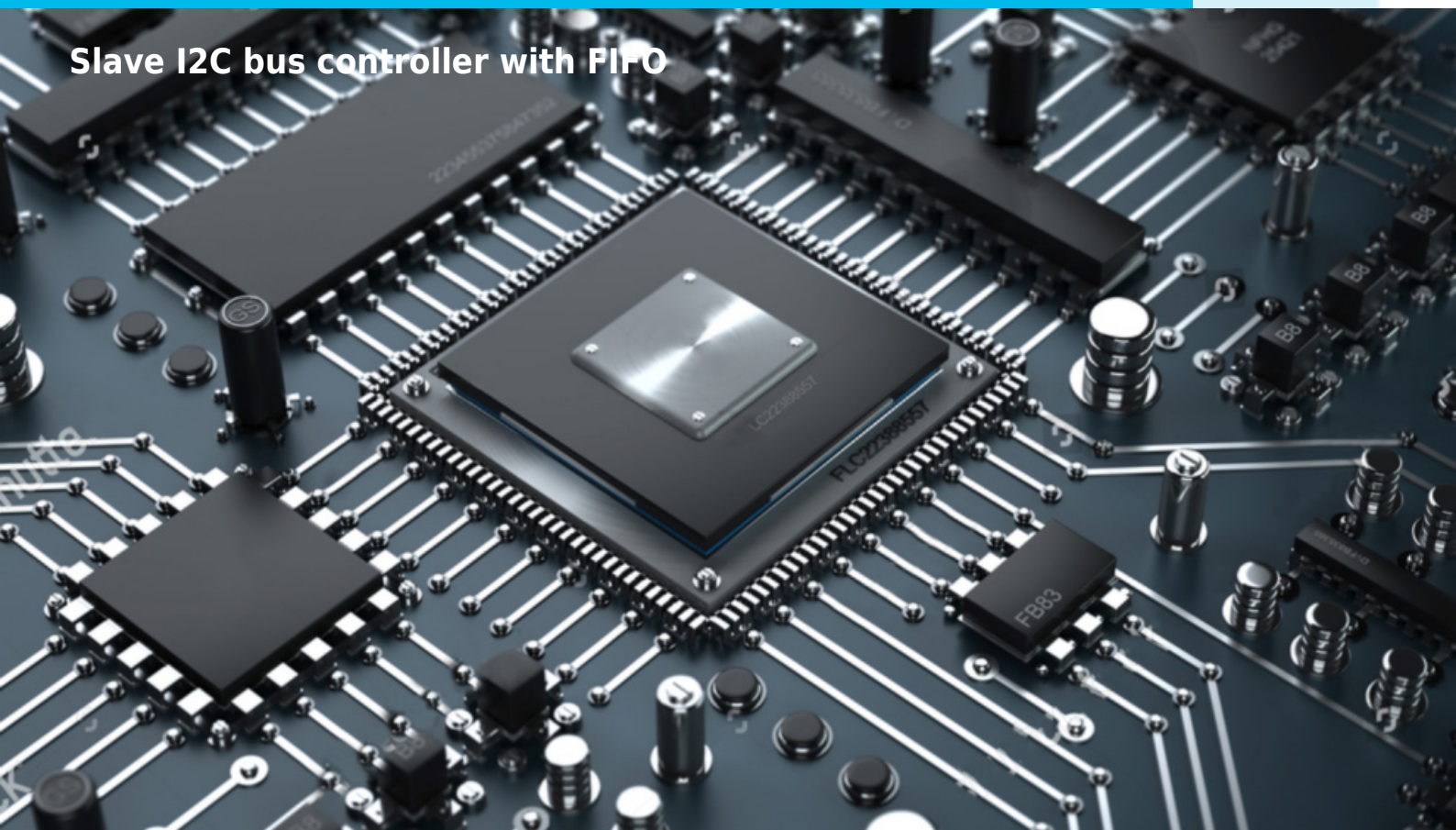
DIGITAL CORE DESIGN

DI2CS

Slave I2C bus controller with FIFO



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DI2CS bridge to APB, AHB, AXI bus, provides an interface between a microprocessor / microcontroller and I2C bus. It can work as:

- a slave transmitter or
- slave receiver

depending on a working mode determined by the master device. The DI2CS core **incorporates all features required by the latest I2C specification**, including:

- clock synchronization,
- arbitration,
- high-speed transmission mode.

The **DI2CS supports all transmission speed modes:**

- Standard (up to 100 kb/s)
- Fast (up to 400 kb/s)
- Fast Plus (up to 1 Mb/s)
- High Speed (up to 3,4 Mb/s)

DCD's IP Core is a **technology independent design** and can be implemented in various process technologies.

KEY FEATURES

- Conforms to v.3.0 of the I2C specification
- Slave operation
  - Slave transmitter
  - Slave receiver
- Supports 3 transmission speed modes
  - Standard (up to 100 kb/s)
  - Fast (up to 400 kb/s)
  - Fast Plus (up to 1 Mb/s)
  - High Speed (up to 3,4 Mb/s)
- Double buffering of RX/TX data
- Configurable RX and TX FIFOs up to 256 bytes each
- Configurable length of SCL, SDA lines glitch filtering
- Allows operation from a wide range of input clock frequencies
- Simple interface allows easy connection to microprocessor/microcontroller devices
- Interrupt generation
- User-defined data setup time
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

UNITS SUMMARY

CPU Interface – Performs the interface functions between DI2CS internal blocks and microprocessor. It allows easy connection of the core with the microprocessor/microcontroller system.
Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.
Shift Register – Controls SDA line, performs data and address shifts during the data transmission and reception.
Control Register – Contains five control bits used for performing all types of I^2C Bus transmissions.
Status Register – Contains seven status bits that indicate state of the I^2C Bus and the DI2CS core.
Input Filter – Performs spike filtering.
Synchronization Logic – Performs DI2CS core synchronization.
Clock Stretching – Performs I^2C SCL clock stretching when DI2CS core is not ready for next transmission.

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route (all key features included):

Device	Speed grade	LE/ALM	F_{max}
MERCURY	-5	200	250 MHz
STRATIX	-5	200	260 MHz
CYCLONE	-6	200	220 MHz
APEX II	-7	200	270 MHz
APEX20KC	-7	200	150 MHz
APEX20KE	-1	200	120 MHz
APEX20K	-1	200	90 MHz
ACEX1K	-1	200	107 MHz
FLEX10KE	-1	200	107 MHz
MAX 7000AE	-5	100	96 MHz
MAX 3000A	-5	100	104 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Multi-Site license option* – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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