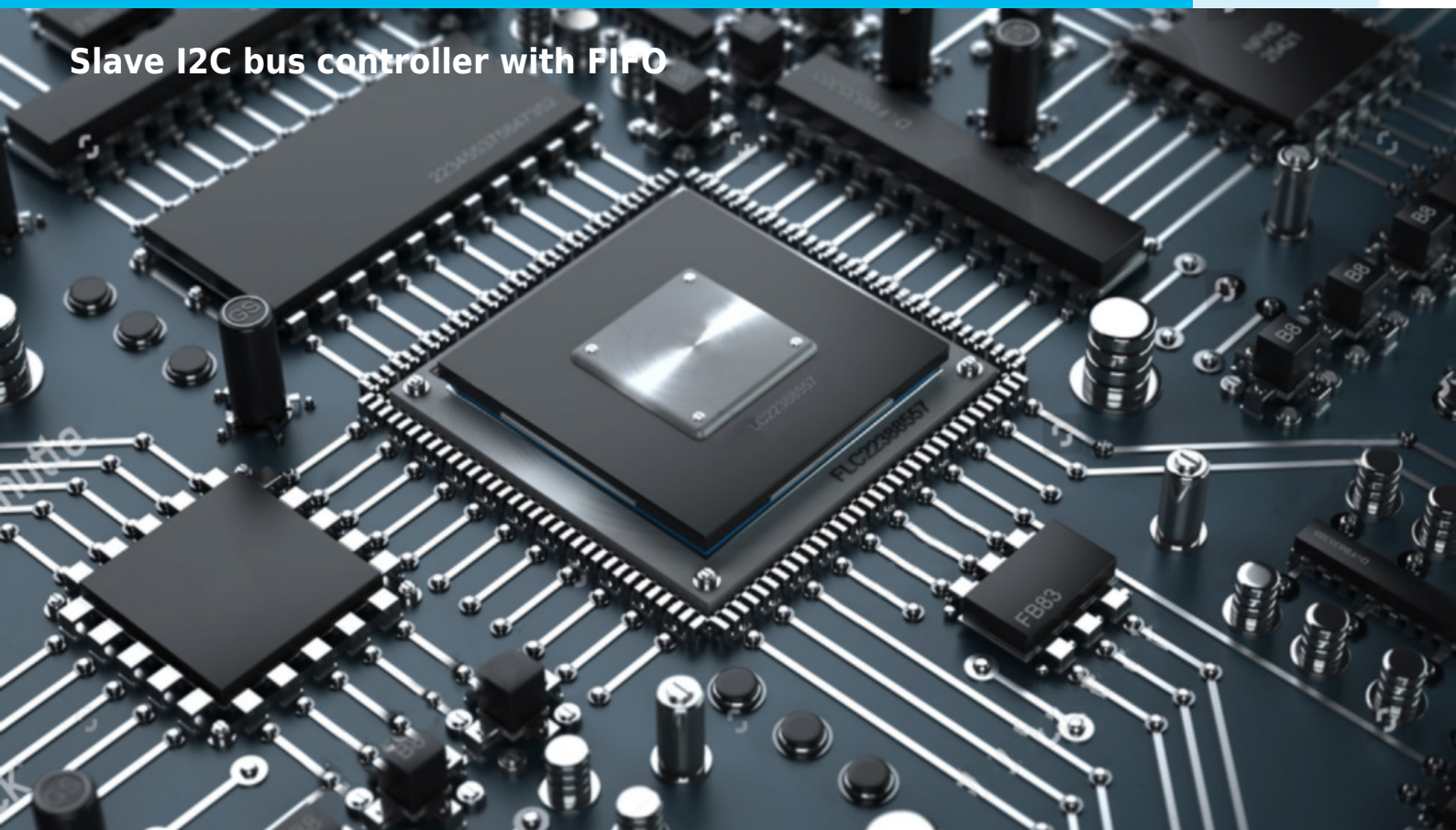
DIGITAL CORE DESIGN

DI2CS

Slave I2C bus controller with FIFO



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DI2CS IP Core – I2C Slave Controller for FPGA & ASIC

The **DI2CS IP Core** from **DCD-SEMI** is a flexible and standards-compliant **I2C slave controller** designed to provide a reliable interface between a **microprocessor or microcontroller** and an **I2C bus** in modern **FPGA and ASIC designs**. Delivered as a scalable **bridge to APB, AHB, and AXI bus architectures**, DI2CS enables seamless integration into a wide range of embedded and SoC platforms.

The core operates exclusively in **slave mode**, functioning as either a **slave transmitter** or **slave receiver**, with the operating role dynamically determined by the **I2C master device** on the bus.

Full Compliance with the Latest I2C Specification

DI2CS incorporates all features required by the **latest I2C specification**, ensuring reliable communication and interoperability with standard-compliant masters. Supported features include:

- **Clock synchronization**
- **Arbitration**
- **High-speed transmission mode**

These capabilities allow the core to operate correctly in both simple and complex I2C system topologies.

Support for All I2C Speed Modes

The DI2CS IP Core supports **all standardized I2C transmission speeds**, making it suitable for a broad range of performance requirements:

- **Standard mode** – up to 100 kb/s
- **Fast mode** – up to 400 kb/s
- **Fast Plus mode** – up to 1 Mb/s
- **High-Speed mode** – up to 3.4 Mb/s

This ensures compatibility with legacy peripherals as well as high-performance I2C systems.

SoC-Friendly and Technology Independent

Designed as a **technology-independent IP Core**, DI2CS can be implemented across multiple **FPGA families and ASIC process technologies**. To support modern SoC architectures, the core can be delivered with:

- **AMBA APB interface**
- **AMBA AHB interface**
- **AMBA AXI interface**

This flexibility allows DI2CS to be easily integrated into both **deeply embedded designs** and **high-end SoC platforms**.

Typical Applications

- I2C peripheral and device emulation
- Sensor and actuator interfaces
- System monitoring and control
- Industrial and consumer electronics
- FPGA-based SoCs requiring I2C slave functionality

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

KEY FEATURES

- Conforms to v.3.0 of the I2C specification
- Slave operation
  - Slave transmitter
  - Slave receiver
- Supports 3 transmission speed modes
  - Standard (up to 100 kb/s)

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- Fast (up to 400 kb/s)
- Fast Plus (up to 1 Mb/s)
- High Speed (up to 3,4 Mb/s)

- Double buffering of RX/TX data
- Configurable RX and TX FIFOs up to 256 bytes each
- Configurable length of SCL, SDA lines glitch filtering
- Allows operation from a wide range of input clock frequencies
- Simple interface allows easy connection to microprocessor/microcontroller devices
- Interrupt generation
- User-defined data setup time
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

UNITS SUMMARY

CPU Interface – Performs the interface functions between DI2CS internal blocks and microprocessor. It allows easy connection of the core with the microprocessor/microcontroller system.
Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.
Shift Register – Controls SDA line, performs data and address shifts during the data transmission and reception.
Control Register – Contains five control bits used for performing all types of I^2C Bus transmissions.
Status Register – Contains seven status bits that indicate state of the I^2C Bus and the DI2CS core.
Input Filter – Performs spike filtering.
Synchronization Logic – Performs DI2CS core synchronization.
Clock Stretching – Performs I^2C SCL clock stretching when DI2CS core is not ready for next transmission.

PERFORMANCE

The following table gives a survey about the Core area and performance in **AMD FPGA** devices after Place & Route (all key features included):

Family	Device	Speed grade	LUT	Slice	F_{max}
Spartan-3	xc3s50	-5	177	122	189 MHz
Spartan-3E	xc3s100e	-5	177	122	189 MHz
Spartan-6	xc6slx4	-3	134	51	286 MHz
Virtex-4	xc4vfx12	-12	204	120	337 MHz
Virtex-5	xc5vlx20t	-2	133	48	443 MHz
Virtex-6	xc6vlx75t	-3	134	57	400 MHz
Virtex-7	xc7vx330t	-3	169	81	494 MHz
Kintex-7	xc7k70t	-3	169	75	536 MHz
Artix-7	xc7a100t	-3	133	49	366 MHz
Virtex UltraScale	xcvu065	-3	121	22	500 MHz
Zynq-7000	xc7z010	-3	128	44	450 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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