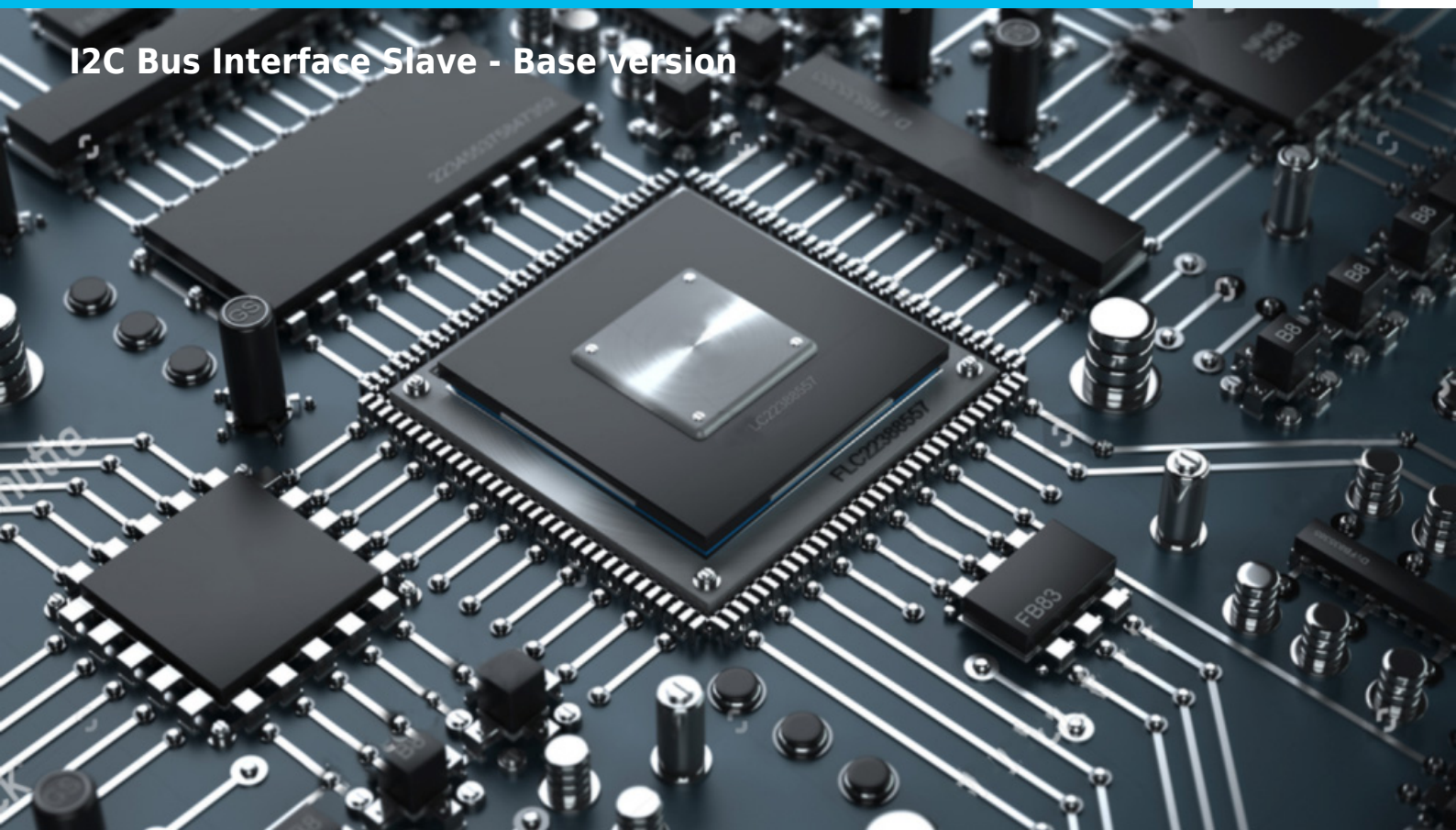
DIGITAL CORE DESIGN

DI2CSB

I2C Bus Interface Slave - Base version



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DI2CSB bridge to APB, AHB, and AXI bus, provides an interface between a passive target device e.g. memory, LCD display, pressure sensors, etc., and the I2C bus. It can work as:

- a slave receiver or
- transmitter

depending on a working mode determined by the master device. A **very simple interface,** composed of reading, write, and data signals, allows **easy connection to target devices**. The core **does not require any programming and is ready to work after power-up/reset**. Read, write, burst read, burst write and repeated start transmissions are automatically recognized by the core. The solution incorporates all features required by the I2C specification. The DI2CSB supports the following **transmission modes:**

- **Standard,**
- **Fast,**
- **Fast Plus,**
- **High Speed.**

The DI2CS is a **technology-independent design** and can be implemented in various process technologies.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.

- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

KEY FEATURES

- Conforms to the latest I2C specification
- Slave operation
  - Slave transmitter
  - Slave receiver
- Supports 3 transmission speed modes
  - Standard (up to 100 kb/s)
  - Fast (up to 400 kb/s)
  - Fast Plus (up to 1 Mb/s)
  - High Speed (up to 3,4 Mb/s)
- Allows operation from a wide range of input clock frequencies
- Support for reads, writes, burst reads, burst writes, and repeated start
- 7-bit addressing
- **No programming required**
- Simple interface allows easy connection to target device e.g. memory, LCD display, pressure sensors etc.
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

UNITS SUMMARY

Target device Interface – Performs the interface functions between DI2CSB internal blocks and target device. Allows easy connection of the core with passive devices e.g. memory, LCD display, pressure sensors, I/O devices etc.
Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.
Shift Register – Controls SDA line, performs data and address shifts, during the data transmission and reception.
Input Filter – Performs spike filtering.
Synchronization Logic – Synchronizes data and address shifts, during the data transmission and reception. SCLI spikes are filtered by this unit.

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PERFORMANCE

The following table gives a survey about the Core area and performance in **LATTICE®** devices after Place & Route (all key features included):

Device	Speed grade	LUTs/PFUs	F_{max}
SC	-7	76 / 42	323 MHz
ECP2	-7	78 / 42	317 MHz
ECP2M	-7	70 / 27	318 MHz
XP2	-7	70 / 27	263 MHz
EC	-5	118 / 27	203 MHz
ECP	-5	118 / 27	212 MHz
XP	-5	118 / 27	180 MHz
ispXPGA	-5	79 / 21	180 MHz
ORCA 4	-3	90 / 15	129 MHz
ORCA 3	-7	73 / 17	84 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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