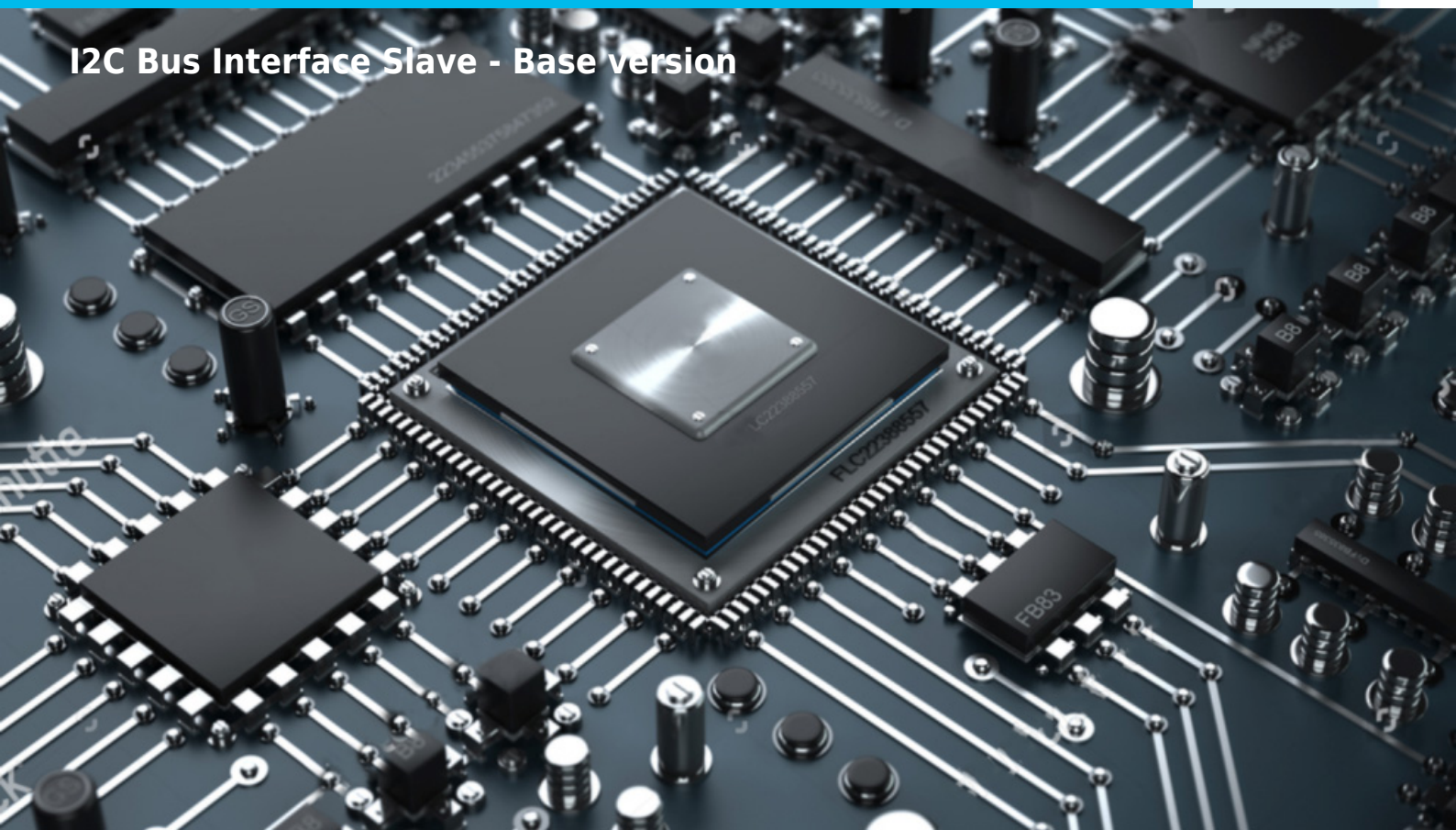
DIGITAL CORE DESIGN

DI2CSB

I2C Bus Interface Slave - Base version



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DI2CSB IP Core – I2C Slave Bridge for Passive Devices in FPGA & ASIC

The **DI2CSB IP Core** from **DCD-SEMI** is a lightweight and efficient **I2C slave bridge** designed to connect **passive target devices**—such as memories, LCD displays, pressure sensors, and other peripherals—directly to an **I2C bus** in **FPGA and ASIC designs**. Delivered as a flexible **bridge to APB, AHB, and AXI bus architectures**, DI2CSB enables rapid and low-complexity integration of I2C-connected devices into modern SoC platforms.

The core operates as either a **slave receiver** or **slave transmitter**, with the operating mode automatically determined by the **I2C master** on the bus.

Zero-Configuration, Ready-to-Use Operation

A key advantage of the DI2CSB IP Core is its **programming-free operation**. The core requires **no software configuration** and is fully operational **immediately after power-up or reset**, making it ideal for simple, cost-sensitive, and low-power designs.

A **very simple target interface**, consisting only of **read, write, and data signals**, allows easy and direct connection to passive devices without complex control logic.

Automatic I2C Transaction Handling

DI2CSB automatically recognizes and handles standard I2C transactions, including:

- **Read and write operations**
- **Burst read and burst write**
- **Repeated start conditions**

All required protocol handling is performed in hardware, minimizing system complexity and CPU involvement.

Full I2C Specification Compliance

The DI2CSB IP Core incorporates all features required by the **I2C specification** and supports all standardized transmission modes:

- **Standard mode** – up to 100 kb/s
- **Fast mode** – up to 400 kb/s
- **Fast Plus mode** – up to 1 Mb/s
- **High-Speed mode** – up to 3.4 Mb/s

This ensures full compatibility with both legacy and high-performance I2C masters.

Technology-Independent and SoC-Friendly

Designed as a **technology-independent IP Core**, DI2CSB can be implemented across a wide range of **FPGA and ASIC process technologies**. For seamless SoC integration, the core can be delivered with:

- **AMBA APB interface**
- **AMBA AHB interface**
- **AMBA AXI interface**

Typical Applications

- Memory devices on I2C bus
- LCD and display controllers
- Sensor interfaces (pressure, temperature, environmental)
- Simple peripheral emulation
- FPGA-based SoCs requiring low-overhead I2C slave connectivity

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

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KEY FEATURES

- Conforms to the latest I2C specification
- Slave operation
  - Slave transmitter
  - Slave receiver
- Supports 3 transmission speed modes
  - Standard (up to 100 kb/s)
  - Fast (up to 400 kb/s)
  - Fast Plus (up to 1 Mb/s)
  - High Speed (up to 3,4 Mb/s)
- Allows operation from a wide range of input clock frequencies
- Support for reads, writes, burst reads, burst writes, and repeated start
- 7-bit addressing
- **No programming required**
- Simple interface allows easy connection to target device e.g. memory, LCD display, pressure sensors etc.
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready

APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

UNITS SUMMARY

Target device Interface – Performs the interface functions between DI2CSB internal blocks and target device. Allows easy connection of the core with passive devices e.g. memory, LCD display, pressure sensors, I/O devices etc.
Control Logic – Manages execution of all commands sent via interface. Synchronizes internal data flow.
Shift Register – Controls SDA line, performs data and address shifts, during the data transmission and reception.
Input Filter – Performs spike filtering.
Synchronization Logic – Synchronizes data and address shifts, during the data transmission and reception. SCLI spikes are filtered by this unit.

PERFORMANCE

The following table gives a survey about the Core area and performance in **LATTICE FPGA** devices after Place & Route (all key features included):

Device	Speed grade	LUTs/PFUs	F_{max}
SC	-7	76 / 42	323 MHz
ECP2	-7	78 / 42	317 MHz
ECP2M	-7	70 / 27	318 MHz
XP2	-7	70 / 27	263 MHz
EC	-5	118 / 27	203 MHz
ECP	-5	118 / 27	212 MHz
XP	-5	118 / 27	180 MHz
ispXPGA	-5	79 / 21	180 MHz
ORCA 4	-3	90 / 15	129 MHz
ORCA 3	-7	73 / 17	84 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

DCD-SEMI Sp. z o.o. Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/

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