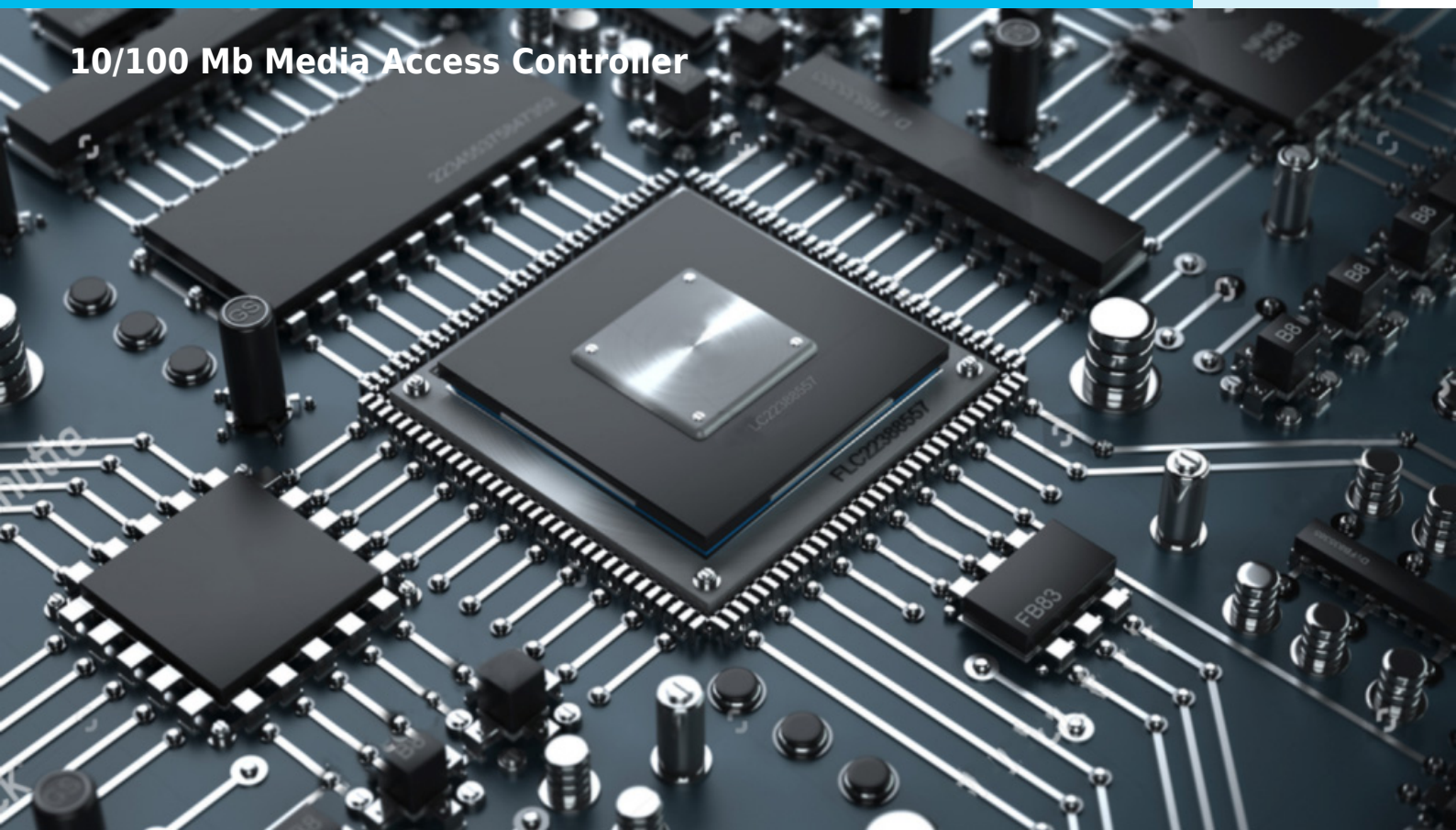
DIGITAL CORE DESIGN

# DMAC

10/100 Mb Media Access Controller



## COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

## IP CORE OVERVIEW

# DMAC IP CORE — IEEE 802.3 ETHERNET MAC BRIDGE FOR EMBEDDED SYSTEMS

### High-Performance Ethernet MAC Bridge for APB, AHB, and AXI Buses

The **DMAC IP Core** from Digital Core Design (DCD-SEMI) is a **hardware implementation of the IEEE 802.3 media access control (MAC) protocol**, providing robust Ethernet connectivity for embedded systems, SoCs, and FPGA designs. Combining **innovation with standardization**, this IP Core ensures reliable **network functionality** when paired with an external PHY device, enabling seamless **transmission and reception of Ethernet frames**.

### Key Features

- **IEEE 802.3-compliant MAC protocol** for standardized Ethernet communication
- Supports **10/100 Mbps speeds** in **half- and full-duplex modes**
- Compatible with **8-, 16-, and 32-bit processors**
- Supports both **little-endian and big-endian byte formats**
- **Static PHY IC configuration** for simplified integration
- **Technology-independent design** deployable across FPGA, ASIC, and SoC technologies
- Ideal for **embedded systems, IoT devices, automotive networks, and industrial applications**

### Why Choose DCD-SEMI DMAC IP Core

- Seamlessly bridges **APB, AHB, and AXI buses** with Ethernet networks
- Fully compatible with a wide range of **processor architectures**
- Provides **high-speed, reliable, and standards-compliant Ethernet connectivity**
- **Flexible integration** into FPGA, ASIC, and SoC designs
- Supports **full- and half-duplex communication** at 10 or 100 Mbps

**DCD-SEMI's DMAC IP Core** enables engineers to implement **robust, high-performance Ethernet functionality** in embedded and industrial designs while ensuring full **IEEE 802.3 compliance**.

**ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.**

For technical specifications or custom configurations, contact **info@dcd-semi.com**

## KEY FEATURES

- Conforms to IEEE 802.3-2002 specification
- Configurable width CPU interface with little or big endianess:
  - 8-bit
  - 16-bit
  - 32-bit
- Simple interface allows easy connection to CPU
- Narrow address bus (4 bits) with indirect I/O interface for transmitted and received data dual port memories
- Supports 10BASE-T and 100BASE-TX/FX IEEE 802.3 compliant MII PHYs
- Media Independent Interface (MII) for connection to external 10/100 Mbps PHY transceivers
- Supports full and half duplex operation at 10 Mbps or 100 Mbps
- CRC-32 algorithm:
  - calculates the FCS nibble at a time
  - automatic FCS generation and checking
  - able to capture frames with CRC errors if required
- Dynamic PHY configuration by STA management interface
- Early receive and transmit interrupts to increase data throughput
- Programmable MAC address
- Promiscuous mode support
- Allows operation from a wide range of input bus clock frequencies
- Fully synthesizable

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- Static synchronous design
- Positive edge clocking
- No internal tri-states
- Lite design, small gate count and fast operation
- Scan test ready

## UNITS SUMMARY

**Transmit module** – Performs transmit management functions, sends frames to Ethernet medium.
**Receive module** – is responsible for receiving frames from the Ethernet. Provides necessary functions for frame decapsulation, CRC checking, address recognizing and error detection.
**Synchronization logic** – There are 3 clock domains in the DMAC core – this module performs synchronization between them.
**TX RAM / RX FIFO RAM interfaces** – Interfaces to external dual port memories used by the DMAC core, to store received and transmitted frames.
**Control and I/O logic** – This module provides interface to CPU/BUS. It exchanges data and control logic with transmit and receive modules, thus controls these, to perform transmit and receive operations.
**STA** – Station Management entity, enables communication with PHY, via simple serial management interface.

## PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** devices (all key features included):

| Component | Area | |
|---|---|---|
| | [gates] | [FFs] |
| RX | 2200 | 172 |
| RX FIFO | 1100 | 131 |
| TX | 2400 | 197 |
| Control & I/O logic | 1500 | 202 |
| STA | 600 | 53 |
| **Total area** | 7800 | 755 |

| Device | Speed | Min area | $F_{max}$ [MHz] clk / txclk / rxclk |
|---|---|---|---|
| 0.25 um | typical | 7800 gates | 250 / >50 / >50 |
| 0.18 um | typical | 7800 gates | 360 / >50 / >50 |
| 0.09 um | typical | 6400 gates | 800 / >50 / >50 |
| 0.06 um | typical | 6300 gates | 900 / >50 / >50 |

rxclk, txclk – design clock is 25 MHz

## APPLICATIONS

- Embedded microprocessor boards
- Networking devices (Network Interface Cards, routers, switches)
- Communication systems

## DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

## LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
***– Single-Site license option*** – dedicated to small and middle sized companies which run their business at one place.
***– Remote Access license option*** – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

## CONTACT

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