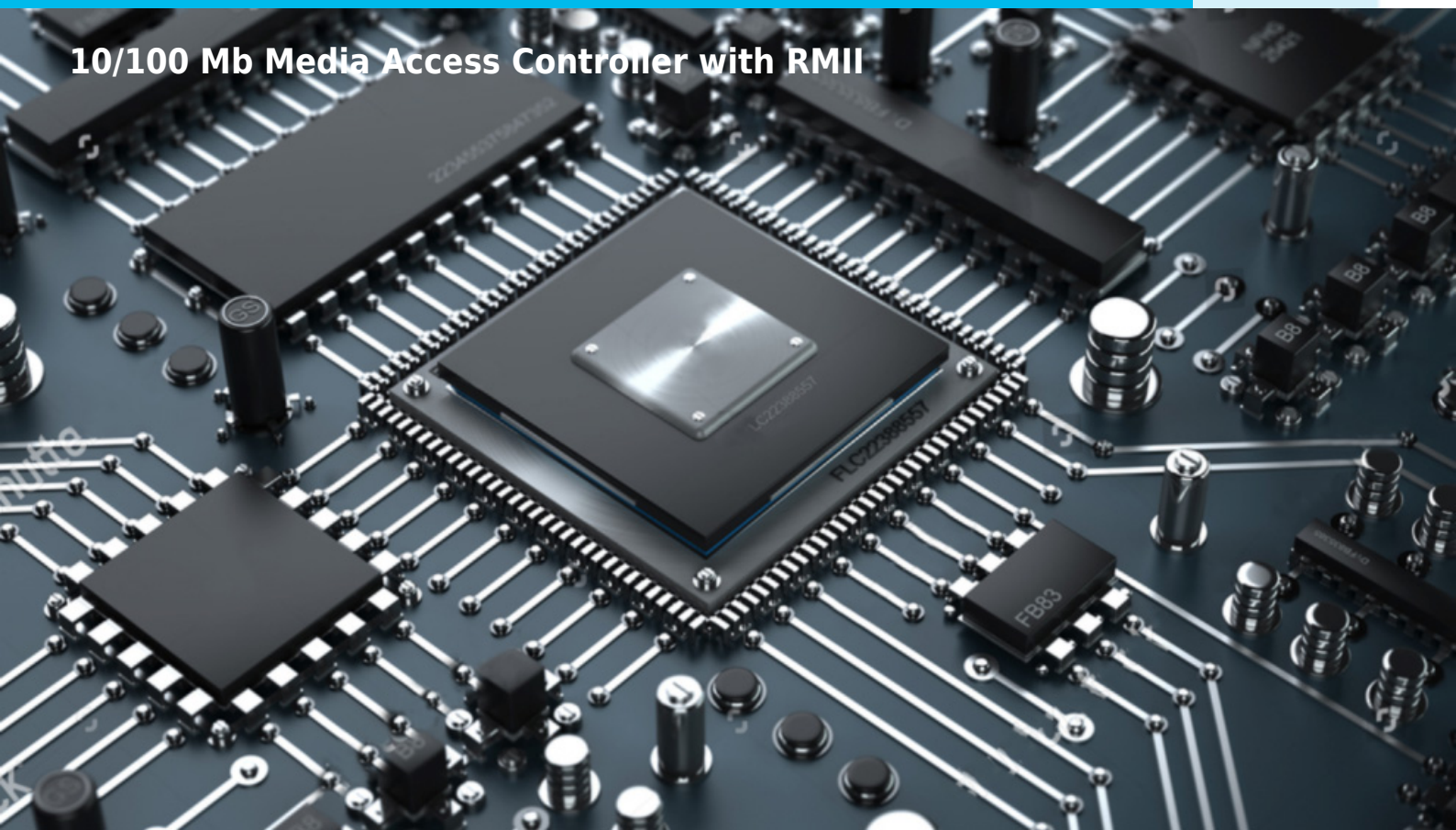
DIGITAL CORE DESIGN

DMAC-RMII

10/100 Mb Media Access Controller with RMII



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DMAC-RMII IP CORE — HIGH-PERFORMANCE ETHERNET MAC BRIDGE FOR EMBEDDED SYSTEMS

Hardware Implementation of IEEE 802.3 Ethernet MAC Protocol

The **DMAC-RMII IP Core** from DCD-SEMI is an **innovative hardware solution** bridging **APB, AHB, and AXI buses** with **Ethernet RMII interfaces**. Designed for embedded systems, SoCs, and FPGA applications, this IP Core enables full **network functionality** in conjunction with an external PHY device, allowing seamless **transmission and reception of Ethernet frames**.

Key Features

- **IEEE 802.3-compliant MAC protocol** for robust Ethernet communication
- Supports **10/100 Mbit/s speeds** in **half- and full-duplex modes**
- Compatible with **8-, 16-, and 32-bit processors**
- Handles both **little-endian and big-endian byte formats**
- Provides **static PHY IC configuration** for simplified integration
- **Technology-independent design**, deployable across multiple process technologies
- Ideal for **embedded systems, IoT devices, automotive networks, and industrial applications**

Why Choose DCD-SEMI DMAC-RMII IP Core

- Seamless **bridge between processor buses and Ethernet networks**
- Supports a wide range of **processor architectures** and data bus widths
- Fully compatible with **IEEE 802.3 standards**
- **Flexible and technology-agnostic design** for ASIC, FPGA, and SoC integration
- Reliable **full/half duplex communication** at 10 or 100 Mbps

Enable fast, reliable, and standards-compliant Ethernet connectivity in your embedded designs with DCD-SEMI's DMAC-RMII IP Core.

Watch the DMAC-RMII presentation on DCD's YouTube:

As Seen On YouTube

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For detailed specifications, integration support, or customization, contact **info@dcd-semi.com**

KEY FEATURES

- Conforms to IEEE 802.3-2002 specification
- Configurable width CPU interface with little or big endianess:
  - 8-bit
  - 16-bit
  - 32-bit
- Simple interface allows easy connection to CPU
- Narrow address bus (4 bits) with indirect I/O interface for transmitted and received data dual port memories
- Supports 10BASE-T and 100BASE-TX/FX IEEE 802.3 compliant MII PHYs
- Reduced Media Independent Interface (RMII) for connection to external 10/100 Mbps PHY transceivers
- Supports full and half duplex operation at 10 Mbps or 100 Mbps
- CRC-32 algorithm:
  - calculates the FCS nibble at a time
  - automatic FCS generation and checking
  - able to capture frames with CRC errors if required
- Dynamic PHY configuration by STA management interface
- Early receive and transmit interrupts to increase data throughput

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- Programmable MAC address
- Promiscuous mode support
- Allows operation from a wide range of input bus clock frequencies
- Fully synthesizable
- Static synchronous design
- Positive edge clocking
- No internal tri-states
- Lite design, small gate count and fast operation
- Scan test ready

UNITS SUMMARY

Transmit module – Performs transmit management functions, sends frames to Ethernet medium.
Receive module – is responsible for receiving frames from the Ethernet. Provides necessary functions for frame decapsulation, CRC checking, address recognizing and error detection.
Synchronization logic – There are 3 clock domains in the DMAC-RMII core – this module performs synchronization between them.
TX RAM / RX FIFO RAM interfaces – Interfaces to external dual port memories used by the DMAC-RMII core, to store received and transmitted frames.
Control and I/O logic – This module provides interface to CPU/BUS. It exchanges data and control logic with transmit and receive modules, thus controls these, to perform transmit and receive operations.
STA – Station Management entity, enables communication with PHY, via simple serial management interface.

APPLICATIONS

- Embedded microprocessor boards
- Networking devices (Network Interface Cards, routers, switches)
- Communication systems

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA** devices after Place & Route (all key features included):

Device	Speed grade	LE/ALM	F_{max} [MHz] clk / rmiiclk
STRATIX IV	-1	896 + 4 kB RAM	420 / 350
STRATIX III	-2	898 + 4 kB RAM	400 / 350
STRATIX II	-3	892 + 4 kB RAM	300 / 260
CYCLONE IV	-6	1 341 + 4 kB RAM	200 / 200
CYCLONE III	-6	1 342 + 4 kB RAM	190 / 190
CYCLONE II	-6	1 340 + 4 kB RAM	158 / 170
STRATIX GX	-5	1 255 + 4 kB RAM	152 / 138
STRATIX	-5	1 255 + 4 kB RAM	162 / 137
CYCLONE	-6	1 254 + 4 kB RAM	148 / 133
APEX II	-7	1 622 + 4 kB RAM	145 / 111
APEX20KC	-7	1 622 + 4 kB RAM	127 / 117
APEX20KE	-1	1 622 + 4 kB RAM	108 / 111
APEX20K	-1	1 622 + 4 kB RAM	86 / 88

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Remote Access license option* – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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