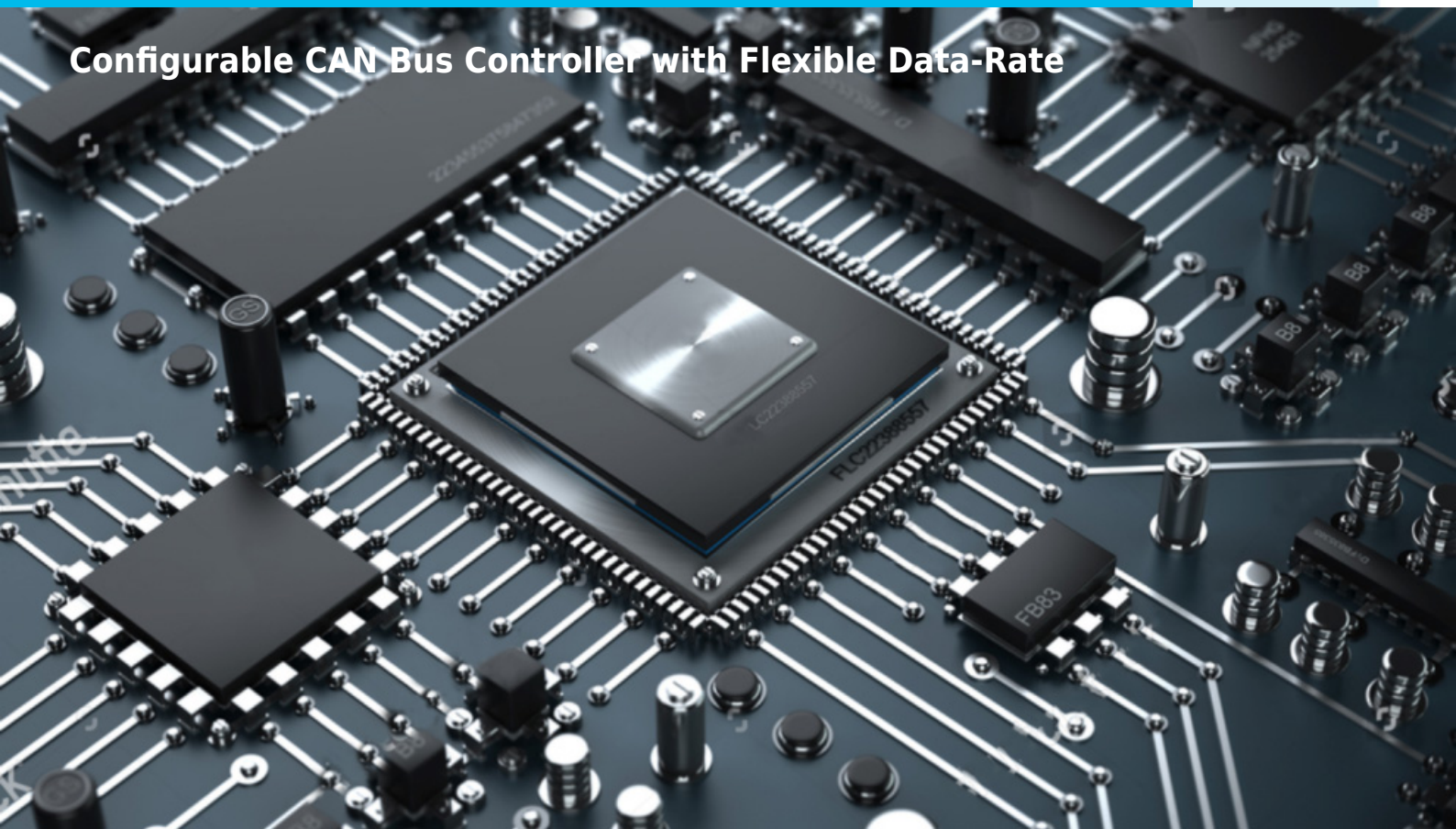


CAN ALL



Configurable CAN Bus Controller with Flexible Data-Rate



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

CAN ALL IP Core is an automotive **COMBO**. Starting from CAN 2.0, CAN FD, CAN FD Full, CAN XL

DCAN FD bridge to APB, AHB, AXI bus, it is a standalone controller for the Controller Area Network (CAN), widely used in automotive and industrial applications. The DCAN FD was designed in accordance with **ISO 11898-1:2015** and conforms to:

- **Bosch CAN 2.0B** specification (2.0B Active) and
- **CAN FD** (flexible data-rate).

Sophisticated error detection functions (which increase communication reliability) and unique fault confinement (which guarantees network-wide data consistency) has decided about CAN's popularity. Because of its fundamental role in all aspects of security and safety, trustworthy implementations are crucial. That's why DCD-SEMI developed a unique IP Core, which **delimits the highest quality standards**. The improved **protocol overcomes standard CAN limits**: data can be transmitted faster than with 1 Mbit/s and the payload (data field) is up to 64 bytes long and limited to 8 bytes anymore. When only one node is transmitting, the bit rate can be increased, because no nodes need to be synchronized. Of course, before the transmission of the ACK slot bit, the nodes need to be re-synchronized. The core has a **simple CPU interface** (8/16/32 bit configurable data width), with a small or big-endian addressing scheme. Hardware message filtering (32 filters) and 128 bytes receive FIFO enable back-to-back message reception, with **minimum CPU load**. The DCAN FD is provided as HDL source code, allowing target use in FPGA and ASIC technologies.

The IP core is available in two versions - Basic and Safety-Enhanced.

This sophisticated solution's been developed as **ISO26262-10 Safety Element out of Context**. It can optionally be improved by necessary safety mechanisms and provide detailed safety documentation: all **ISO26262 soft IP SEooC** required work products, which include complete **Failure Modes Effects and Detection Analysis FMEDA** analysis with step by step instruction to help to integrate the IP into the customer's system and to conduct the system-level

safety analysis. All the safety-related work products were checked by a third-party, independent audit.

The conducted safety analysis depicts, that the safety metrics are fulfilled and both IPs reach the Automotive Safety Integrity Level ASIL-B (**Single Point Fault Metric SPFM > 90%**, **Latent Fault Metric LFM > 60%**). DCD-SEMI delivers a complete **FMEDA analysis** with step-by-step instruction to help to integrate the IP into the customer's system and to conduct the system-level safety analysis.

This **ASIL-B ready design** may easily be used in **Automotive Safety Systems at the ASIL-B level**, but DCD-SEMI may optionally deliver higher ASIL level ready IP. For further information and the optional features please contact our support.

CAN FuSa white papers

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- **Altera / Intel,**
- **Xilinx / AMD,**
- **Lattice,**
- **Microsemi / Microchip,**
and others.
- **TSMC**
- **UMC**
- **SK Hynix**
and others.

KEY FEATURES

- Designed in accordance to **ISO 11898-1:2015**
- Supports **CAN 2.0B** and **CAN FD** frames
- Support up to 64 bytes data frames
- **Flexible data-rates supported**
- Supports emotas CANopen FD stack
- 8/16/32-bit CPU slave interface with small or big endianness
- Simple interface allows easy connection to CPU
- Supports both standard (11-bit identifier) and extended (29 bit identifier) frames
- **Data rate up to 8 Mbps**
- Hardware message filtering (dual/single filter)
- 128 byte receive FIFO and transmit buffer
- Overload frame is generated on FIFO overflow
- **Normal & Listen Only Mode**
- Transceiver Delay Compensation up to three data bit long
- Single Shot transmission
- Ability to abort transmission
- Readable error counters
- **Last Error Code**
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states

- Scan test ready
- **Available system interface wrappers:**
- **Available system interface wrappers:**
 - **AMBA - APB / AHB / AXI Lite Bus**
 - **Altera Avalon Bus**
 - **Xilinx OPB Bus**

UNITS SUMMARY

Interface Management Logic (IML) - interprets commands from the CPU, provides interrupt and status indication.

Bit Stream Processor (BSP) - translates messages into frames and vice versa.

Baud Rate Prescaler (BRP) - defines the length of time quantum.

Bit Timing Logic (BTL) - processes the bit time, calculates position of the sample point and performs synchronization.

Error Management Logic (EML) - is responsible for fault confinement handling.

Acceptance Filter (ACF) - decides, whether incoming messages are accepted or not, based on filter registers settings.

TX/RX RAM interfaces - interfaces to external dual port memories used by the DCAN core, to store received and transmitted frames.

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	Speed grade	LE/ALM	Memory bytes
ARRIA V	-6	851	40
CYCLONE V	-8	831	40
STRATIX V	-3	867	40

8-bit CPU Core performance in INTEL FPGA® devices without CAN FD option.

Device	Speed grade	LE/ALM	Memory bytes
ARRIA V	-6	1 385	256
ARRIA 5 SOC	3_H3	1 194	168
ARRIA 10	-1	1 214	302
ARRIA 10 SOC	-2	1 229	262
CYCLONE 5 SOC	-6	1 200	133
CYCLONE 10 LP	-6	2 780	130
CYCLONE 10 GX	-5	1 218	268
STRATIX 5 SOC	-3	1 383	256
STRATIX 10	-1	1 437	292
MAX 10	-6	2 787	134

8-bit CPU Core performance in INTEL FPGA® devices with CAN FD option

DELIVERABLES

- **Source code:**

- VERILOG or VHDL Source Code
- VERILOG or VHDL test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
- Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
 - Synthesis scripts
- **Netlist**
 - Netlist for selected FPGA family
 - Sample FPGA project
 - Technical documentation
 - HDL core specification
 - Datasheet
- **Technical support**
 - IP Core implementation
 - 12 months maintenance
 - Delivery of the IP Core and documentation updates
 - Phone & email support
 - Design consulting

APPLICATIONS

- Automotive, industrial
- Embedded communication systems

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

- **Single-Site license option** - dedicated to small and middle sized companies which run their business at one place.

- **Multi-Site license option** - dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:

- VHDL or Verilog RTL synthesizable source code (called HDL Source code)
- FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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