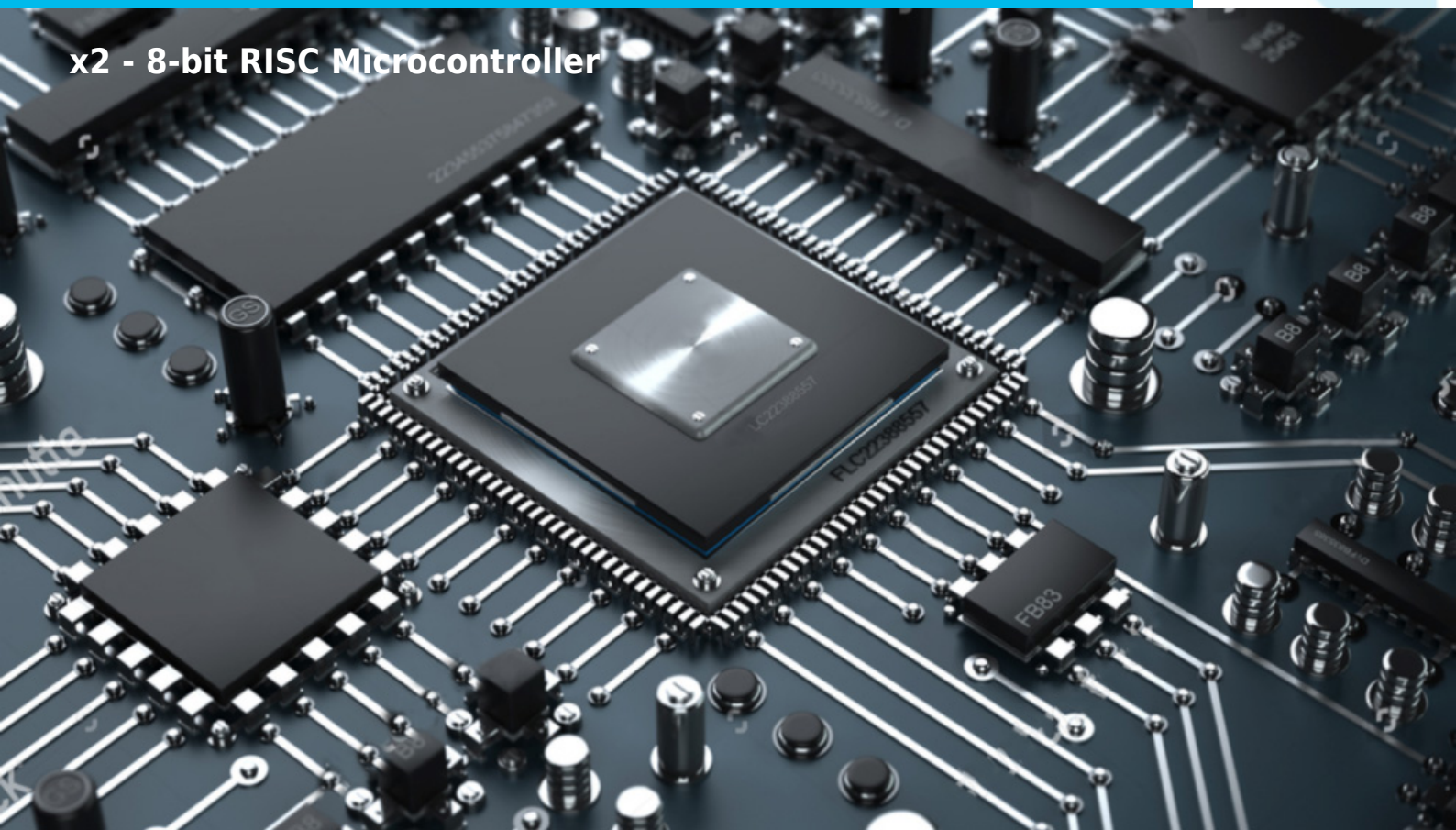
DIGITAL CORE DESIGN

DFPIC165X

x2 - 8-bit RISC Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DFPIC165X 8-Bit PIC Microcontroller IP Core – High-Performance, Low-Power, Fully Customizable

The **DFPIC165X** is a low-cost, high-performance, 8-bit fully static soft IP Core, optimized to operate with fast on-chip memory while maintaining ultra-low power consumption. Fully **software-compatible** with **PIC16C54, PIC16C55, PIC16C56, PIC16C57, and PIC16C58** industry standards, the DFPIC165X delivers enhanced performance and efficiency for embedded applications.

Key Features & Benefits:

- **High-Speed RISC Architecture:** Modified 12-bit instruction RISC core with separate 8-bit data bus achieves 2× faster execution than original PIC16C5X cores, delivering up to 8× speed improvement over comparable 8-bit microcontrollers.
- **Code Efficiency:** Typically achieves 2:1 code compression for compact software footprint.
- **Integrated Peripherals:** 24 general-purpose I/O lines, 8-bit timer/counter with programmable prescaler.
- **Low-Power Operation:** SLEEP mode reduces power consumption; the controller can wake via user reset or watchdog overflow.
- **Watchdog Timer:** Integrated WDT with dedicated clock signal protects against software lock-up.
- **Versatile Applications:** Perfect for high-speed automotive and appliance motor control, low-power remote transmitters/receivers, pointing devices, and telecom processors.
- **Compact Footprint:** Small silicon area usage makes it ideal for space-constrained programmable devices.
- **Full Customization:** Delivered in an exact configuration to meet project-specific requirements, avoiding wasted features and unnecessary silicon.
- **Automated Validation:** Comes with a fully automated test bench and comprehensive verification suite for seamless SoC integration.

DoCD™ Real-Time Hardware Debugging:
Each DFPIC165X core features **DCD's proprietary DoCD™ hardware debugger**, providing **non-intrusive debugging** for the entire SoC. The DoCD™ can halt, run, step into, or skip instructions and access all microcontroller contents, including registers, SFRs, user-defined peripherals, and program/data memories.

Applications: Automotive electronics, low-power embedded systems, telecom devices, motor controllers, battery-operated IoT devices, and general-purpose SoCs requiring high-speed, low-power 8-bit microcontrollers.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

CPU FEATURES

- Software compatible with industry standard PIC16C5X
- Harvard RISC architecture
- 2 times faster, compared to original implementation
- 33 instructions
- 12 bit wide instruction word
- Up to 256 bytes of internal Data Memory
- Up to 4K bytes of Program Memory
- Configurable hardware stack
- Power saving SLEEP mode
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- Technology independent HDL Source Code
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

PERIPHERALS

- **Three 8 bit I/O ports**
  - Three 8-bit corresponding TRIS registers
- **Timer 0**
  - 8-bit timer/counter
  - Readable and Writable
  - 8-bit software programmable prescaler
  - Internal or external clock select
  - Edge select for external clock
- **Watchdog Timer**
  - Configurable Time out period
  - 7-bit software programmable prescaler
  - Dedicated independent Watchdog Clock input

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OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented DFPIC165X Microcontroller Core) are also available. The optional peripherals can be implemented upon customer's request.

- **Full duplex UART**
- **SPI – Master and Slave Serial Peripheral Interface**
- **I2C bus controller – Master**
- **I2C bus controller – Slave**

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs arithmetic and logic operations, during execution of an instruction. This module contains work register (W) and Status register.
Control Unit – It performs the core synchronization and data flow control. This module manages execution of all instructions. Performs decode and control functions for all other blocks. It contains program counter (PC) and hardware stack.
Hardware Stack – The DFPIC165X configurable hardware stack. The stack space is not a part of either program or data space and the stack pointer is not readable or writable. The PC is pushed onto the stack, when CALL instruction is executed or an interrupt causes a branch. The stack is popped during RETLW instruction execution. The stack operates as a circular buffer. This means that after the stack has been pushed two times, the third push overwrites the value that was stored from the first push.
RAM Controller – It performs interface functions between Data memory and DFPIC165X internal logic. It assures correct Data memory addressing and data transfers. The DFPIC165X supports two addressing modes: direct or indirect. In Direct Addressing, the 8-bit direct address is computed from FSR(7:5) bits and from 5 least significant bits of instruction word. Indirect addressing is possible, by using the INDF register. Any instruction using INDF register, actually accesses data pointed to by FSR (file select register). Reading INDF register indirectly, will produce 00h. Writing to the INDF register indirectly, results in a no-operation. An effective 8-bit address is obtained from an 8-bit FSR register.
Timer 0 – Main system's timer and prescaler. The DFPIC165X Timer operates in two modes: 8-bit timer or 8-bit counter. In the "timer mode", timer registers are incremented every 4 CLK periods. When the prescaler is assigned into the TIMER pre-scale ratio can be divided by 2, 4 .. 256. In the "counter mode", the timer register is incremented every falling or rising edge of T0CKI pin, depending on T0SE bit in OPTION register.
Watchdog Timer – it is a free running timer. WDT has own clock input, separate from system clock. It means, that the WDT will run even if the system clock is stopped by execution of SLEEP instruction. During normal operation, a WDT timeout generates a Watchdog reset. If the device is in SLEEP mode, the WDT timeout causes the device to wake up and continue with normal operation.
I/O Ports – Block contains DFPIC165X's general purpose I/O ports and data direction registers (TRIS). The DFPIC165X has three 8-bit full bi-directional ports PORT A, PORT B and PORT C. Read and write accesses to the I/O port are performed via their corresponding SFR's PORTA, PORTB, PORTC. The reading instruction always reads the status of Port pins. Writing instructions always write into the Port latches. Each port's pin has a corresponding bit in TRISA, TRISB and TRISC registers. When the bit of TRIS register is set, this means that the corresponding bit of port is configured as an input (output drivers are set into the High Impedance).

CONFIGURATION

The following parameters of the DFPIC165X core can be easily adjusted to requirements of a dedicated application and technology. The configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

– RAM memory type: *synchronous / asynchronous*
– RAM size: *up to 256 / default 128*
– Program Memory size: *up 4 kWords / default 2k*
– Number of hardware stack levels: *1-8 / default 2*
– SLEEP mode: *used / unused*
– WATCHDOG Timer: *used/width / unused*
– Timer system: *used / unused*
– PORTS A,B,C: *used / unused*

IMPROVEMENT

Most instruction of DFPIC165X is executed within 2 CLK cycles. Except the conditional program memory branches, in case the condition of branch instruction is met. The following table shows sample instructions execution times.

Mnemonic operands	DFPIC165X (CLK cycles)	PIC16C54 (CLK cycles)	Impr.
ADDWF	2	4	2
ANDWF	2	4	2
RLF	2	4	2
BCF	2	4	2
DECFSZ	2(4)[1]	4(8)[1]	2
INCFSZ	2(4)[1]	4(8)[1]	2
BTFSC	2(4)[1]	4(8)[1]	2
BTFSS	2(4)[1]	4(8)[1]	2
CALL	2	8	4
GOTO	2	8	4
RETLW	2	8	4

[1]– number of clock in case that result of operation is 0.

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA** devices after Place & Route:

Device	Speed grade	LE/ALM	F_{max}
CYCLONE	-6	551	105 MHz
CYCLONE II	-6	547	108 MHz
STRATIX	-5	551	108 MHz

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STRATIX II	-3	456	178 MHz
STRATIX GX	-5	551	109 MHz
APEX II	-7	635	73 MHz
APEX20KC	-7	635	68 MHz
APEX20KE	-1	635	56 MHz
APEX20K	-1	635	45 MHz
ACEX1K	-1	648	50 MHz
FLEX10KE	-1	648	48 MHz

*CPU – consisted of ALU, Control Unit, Bus Controller, Hardware Stack, 256 B RAM, 4k of Program memory

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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