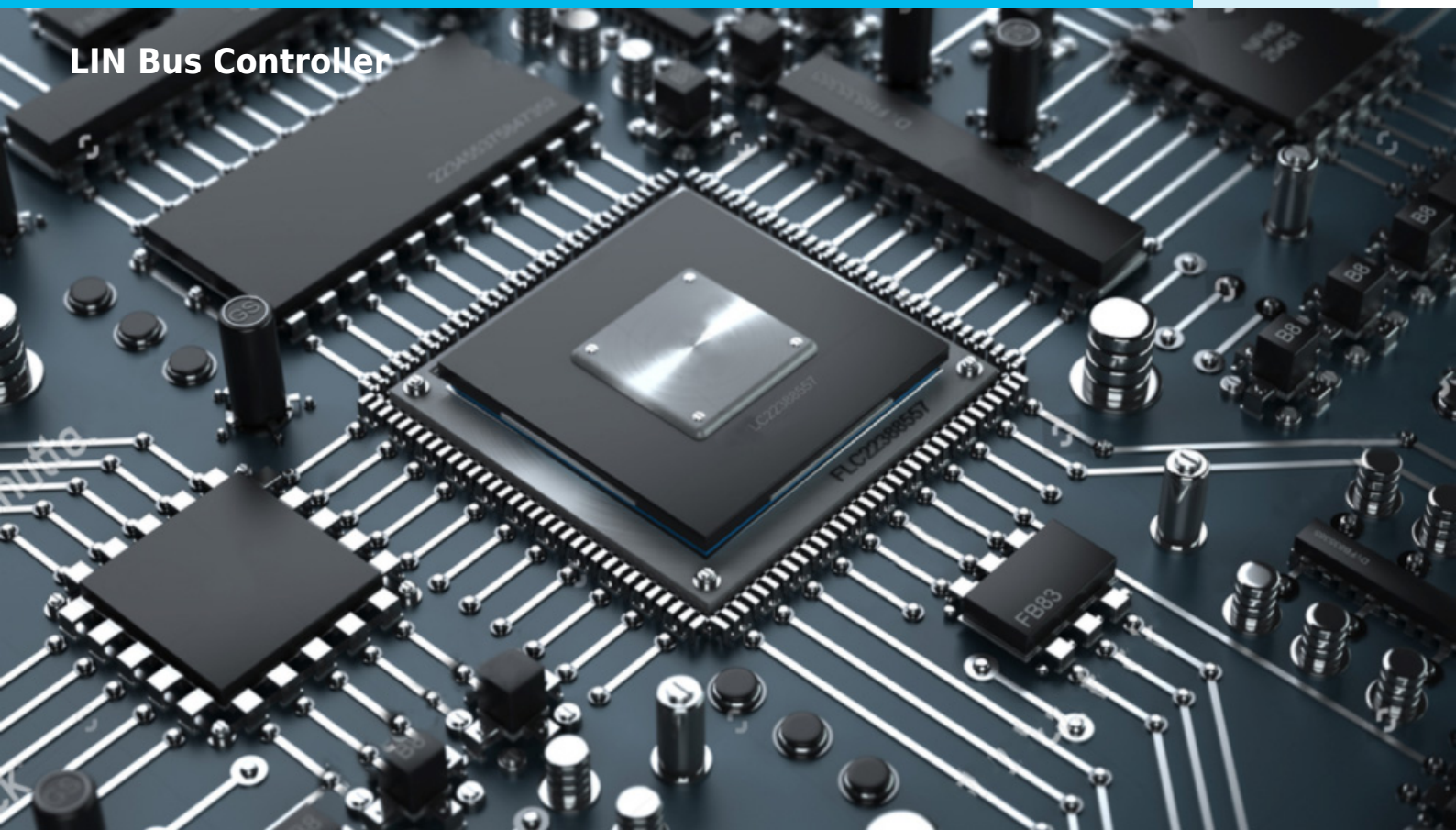
DIGITAL CORE DESIGN

DLIN



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DCD-SEMI believes that even though something may be small or slow, it can still offer **maximal efficiency** and **ultimate reliability**. That's why our DLIN controller supports transmission speed between 1kb/s and 20kb/s, which allows to transmit and receive LIN messages compatible to:

- LIN 1.3,
- LIN 2.1
- and the newest LIN 2.2A

DLIN bridge to APB, AHB, AXI bus, it is a soft core of the Local Interconnect Network (LIN). This interface is a serial communication protocol, primarily designed to be used in automotive applications. Compared to the CAN, The LIN is slower, but **thanks to its simplicity, it is much more cost effective**. Our Core is ideal for communication in intelligent sensors and actuators, where the bandwidth and versatility of the CAN is not required. The **DLIN core provides an interface between a microprocessor/microcontroller and LIN bus**. It can work as a master or slave LIN node, depending on a work mode determined by the microprocessor/microcontroller. DCD's controller **supports transmission speed between 1 and 20kb/s**, which allows it to transmit and receive LIN messages compatible to LIN 1.3., LIN 2.1, and the newest 2.2A specification. The reported information status includes type and condition of transfer operations performed by the DLIN, as well as a wide range of LIN error conditions (overrun, framing, parity, timeout). Our Core includes programmable timer which allows detecting timeout and synchronization error. The DLIN is described at RTL level, empowering the target use in FPGA and ASIC technologies.

Watch the DLIN presentation on DCD's You Tube:

KEY FEATURES

- Conforms with LIN 1.3, LIN 2.1 and LIN 2.2A specification.
- Automatic LIN Header handling
- Automatic Re-synchronization
- Data rate between 1Kbit/s and 20 Kbit/s
- Master and Slave work mode
- Time-out detection
- Extended error detection
- "Break-in-data" support
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Lite Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

UNITS SUMMARY

Host Controller Interface – Accepts inputs from the system bus and generates control signals for other DLIN functional blocks. Address bus ADDR(2:0), selects one of register to be read from/written into. Active level of RD, WR and CS, can be configurable. RD and WR are ignored, unless the DLIN has been selected, by activating CS input. **Control State Unit** – Composed of two state machines, the master and the slave, which control master and slave tasks. The master task handles all bus communication. It must initiate any slave response, by sending out a synch break, a synch field and protected identifier field. Slave task is responsible for sending the response message, if it is addressed by the master. **Baud Rate Generator** – The DLIN contains a programmable 15 bit baud generator, which divides clock input, by a divisor in the range between 1 and (2^{15}-1). The output frequency of the baud generator is 32 x the baud rate. Two registers, called divisor latches DLL and DLH, store the divisor in the 15-bit binary format. **Receiver Control & Shift Register** – Responsible for receiving frame from LIN bus. Provides necessary function for data reception, frame timing and error checking. **Data Buffer** – stores the receive or transmit data. **Transmitter Control & Shift Register** – Performs transmit management function, sends data by LIN bus. **Interrupt Controller** – Works with transmitter, receiver and control unit, to indicate DLIN transmission events or errors. User can configure, which events may generates interrupt by enabled or disabled corresponding bits, in Interrupt Enable register. When interrupt is generated, host can find information about reason by reading LIN Status Register.

APPLICATIONS

- Automotive, industrial
- Embedded communication systems

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** devices, after Place & Route (all key features included):

Device	Speed grade	Area [gates]	F_{max} [MHz]
0.18u speed	typical	4 600	350
0.18u area	typical	4 500	100

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code

- VERILOG or VHDL test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application

- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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