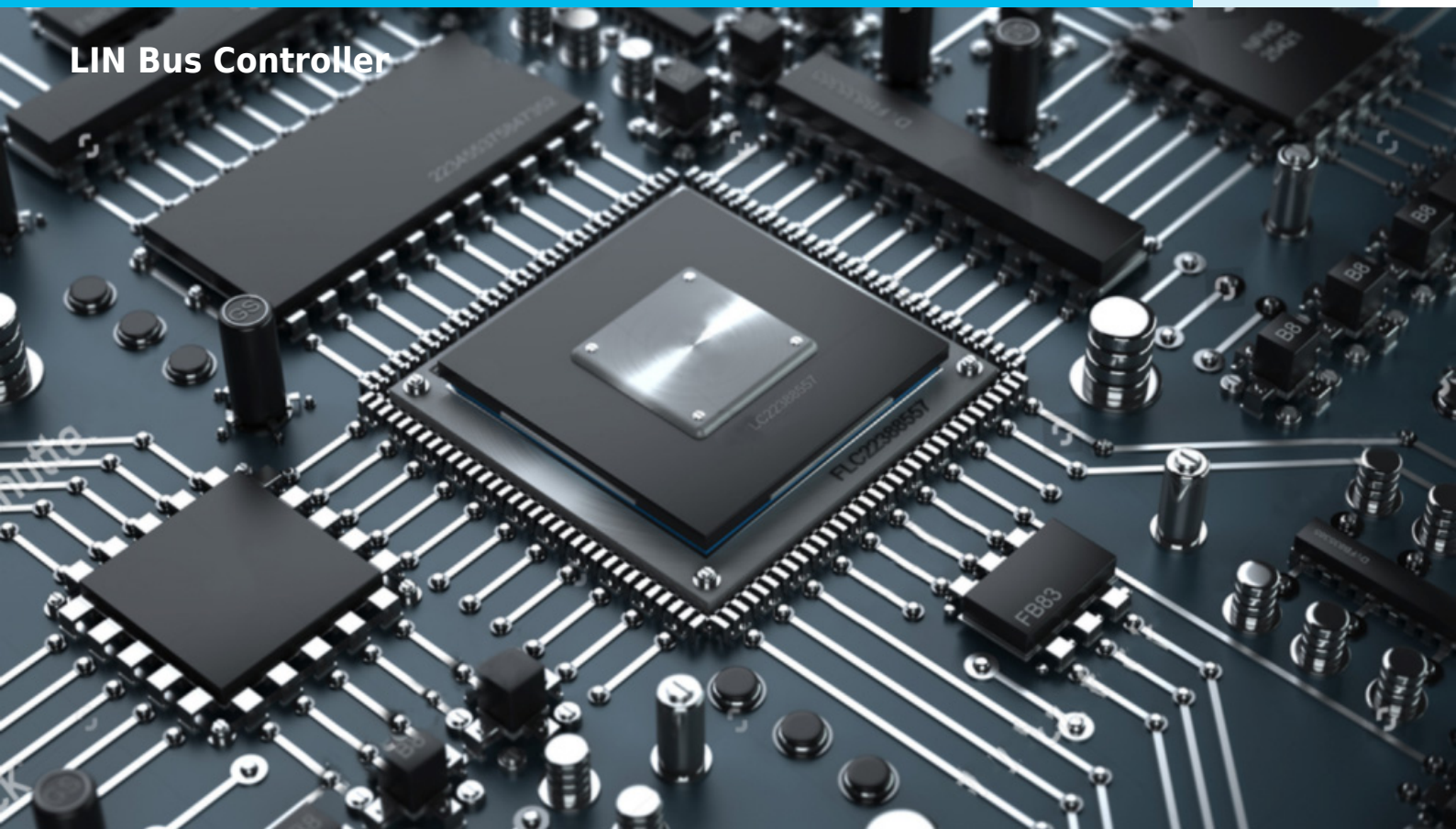


DLIN



LIN Bus Controller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DCD believes that even though something may be small or slow, it can still offer **maximal efficiency** and **ultimate reliability**. That's why our DLIN controller with UART half-duplex enhanced functionality supports transmission speeds between 1kb/s and 20kb/s, which allows us to transmit and receive LIN messages compatible to:

- LIN 1.3,
- LIN 2.1
- and the newest LIN 2.2A

DLIN bridge to APB, AHB, and AXI bus, it is a softcore of the Local Interconnect Network (LIN). This interface is a serial communication protocol, primarily designed to be used in automotive applications. Compared to the CAN, The LIN is slower, but **thanks to its simplicity, it is much more cost-effective**. Our Core is ideal for communication in intelligent sensors and actuators, where the bandwidth and versatility of the CAN is not required. The **DLIN core provides an interface between a microprocessor/microcontroller and a LIN bus**. It can work as a master or slave LIN node, depending on a work mode determined by the microprocessor/microcontroller. DCD's controller **supports transmission speeds between 1 and 20kb/s**, which allows it to transmit and receive LIN messages compatible with LIN 1.3., LIN 2.1, and the newest 2.2A specification. The reported information status includes the type and condition of transfer operations performed by the DLIN, as well as a wide range of LIN error conditions (overrun, framing, parity, timeout). Our Core includes a programmable timer that allows for detecting timeout and synchronization errors. The DLIN is described at the RTL level, empowering the target use in FPGA and ASIC technologies.

The IP core is available in two versions - Basic and Safety-Enhanced.

This sophisticated solution's been developed as **ISO26262-10 Safety Element out of Context**. It can optionally be improved by necessary safety mechanisms and provide detailed safety documentation: all **ISO26262 soft IP SEooC** required work products, which include complete **Failure Modes Effects and Detection Analysis FMEDA** analysis with step-by-step instruction to help to

integrate the IP into the customer's system and to conduct the system-level safety analysis. All the safety-related work products were checked by a third-party, independent audit.

The conducted safety analysis depicts, that the safety metrics are fulfilled and both IPs reach the Automotive Safety Integrity Level ASIL-B (**Single Point Fault Metric SPFM > 90%, Latent Fault Metric LFM > 60%**). DCD-SEMI delivers a complete **FMEDA analysis** with step-by-step instructions to help to integrate the IP into the customer's system and to conduct the system-level safety analysis.

This **ASIL-B ready design** may easily be used in **Automotive Safety Systems at the ASIL-B level**, but DCD-SEMI may optionally deliver higher ASIL level ready IP. For further information and the optional features please contact our support.

LIN FuSa white papers

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- **Altera / Intel,**
- **Xilinx / AMD,**
- **Lattice,**
- **Microsemi / Microchip, and others.**
- **TSMC**
- **UMC**
- **SK Hynix and others.**

KEY FEATURES

- Conforms with LIN 1.3, LIN 2.1 and LIN 2.2A specification
- LIN with UART half-duplex enhanced functionality
- Automatic LIN Header handling
- Automatic Re-synchronization
- Data rate between 1Kbit/s and 20 Kbit/s
- Master and Slave work mode
- Time-out detection
- Extended error detection
- "Break-in-data" support
- **Available system interface wrappers:**
 - **AMBA - APB / AHB / AXI Lite Bus**
 - **Altera Avalon Bus**
 - **Xilinx OPB Bus**

UNITS SUMMARY

Host Controller Interface - Accepts inputs from the system bus and generates control signals for other DLIN functional blocks. Address bus ADDR(2:0), selects one of register to be read from/written into. Active level of RD, WR and CS, can be configurable. RD and WR are ignored, unless the DLIN has been selected, by activating CS input. **Control State Unit** - Composed of two state machines, the master and the slave,

which control master and slave tasks. The master task handles all bus communication. It must initiate any slave response, by sending out a synch break, a synch field and protected identifier field. Slave task is responsible for sending the response message, if it is addressed by the master. **Baud Rate Generator** - The DLIN contains a programmable 15 bit baud generator, which divides clock input, by a divisor in the range between 1 and $(2^{15}-1)$. The output frequency of the baud generator is 32 x the baud rate. Two registers, called divisor latches DLL and DLH, store the divisor in the 15-bit binary format. **Receiver Control & Shift Register** - Responsible for receiving frame from LIN bus. Provides necessary function for data reception, frame timing and error checking. **Data Buffer** - stores the receive or transmit data. **Transmitter Control & Shift Register** - Performs transmit management function, sends data by LIN bus. **Interrupt Controller** - Works with transmitter, receiver and control unit, to indicate DLIN transmission events or errors. User can configure, which events may generate interrupt by enabled or disabled corresponding bits, in Interrupt Enable register. When interrupt is generated, host can find information about reason by reading LIN Status Register.

APPLICATIONS

- Automotive, industrial
- Embedded communication systems

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route (all key features included): MAX5-3331421

Device	Speed grade	LE/ALM	F _{max}
ARRIA GX	-6	501/338	166
ARRIA IIGX	-3	505/337	319
ARRIA V	-6	326	224
ARRIA 5 SOC	3_H3	440	116
ARRIA 10	-2	442	113
ARRIA 10 SOC	-2	441	127
CYCLONE	-6	715	159
CYCLONE2	-6	998	207
CYCLONE3	-6	715	205
CYCLONE4	-6	723	185
CYCLONE5	-8	449	172
CYCLONE5 SOC	-6	440	118
CYCLONE10 GX	-5	450	80
CYCLONE10 LP	-6	992	124
STRATIX	-5	674	147
STRATIXGX	-5	462	184
STRATIX 2	-3	467	266
STRATIX 3	-2	502	392
STRATIX 4	-2	506	409
STRATIX 5	-3	331	421
STRATIX 10	-1	531	128
MAX5	-4	979	82

DELIVERABLES

- **Source code:**
 - VERILOG or VHDL Source Code
 - VERILOG or VHDL test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
 - Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
 - Synthesis scripts
 - Example application
- **Netlist**
 - Netlist for selected FPGA family
 - Sample FPGA project
 - Technical documentation
 - HDL core specification
 - Datasheet
- **Technical support**
 - IP Core implementation
 - 12 months maintenance
 - Delivery of the IP Core and documentation updates
 - Phone & email support
 - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

- **Single-Site license option** - dedicated to small and middle sized companies which run their business at one place.

- **Multi-Site license option** - dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:

- VHDL or Verilog RTL synthesizable source code (called HDL Source code)

- FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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