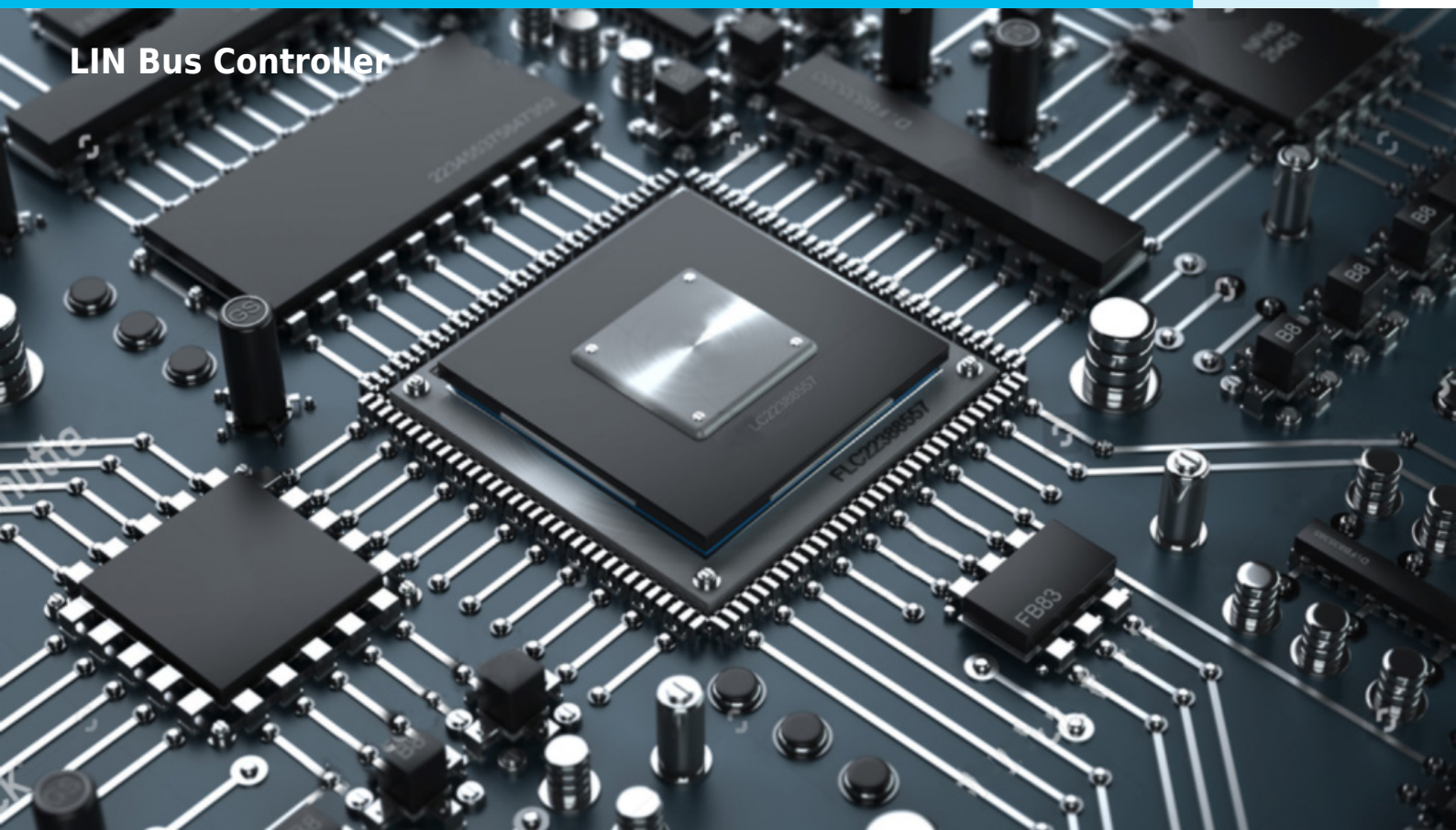
DIGITAL CORE DESIGN

LIN WITH UART



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DLIN IP CORE — EFFICIENT, RELIABLE LIN CONTROLLER FOR AUTOMOTIVE APPLICATIONS

HIGH-EFFICIENCY LIN COMMUNICATION FOR INTELLIGENT SENSORS AND ACTUATORS

The **DLIN IP Core** from DCD-SEMI is a **UART half-duplex enhanced Local Interconnect Network (LIN) controller**, designed to deliver **maximum efficiency and ultimate reliability** even at modest data rates. Supporting transmission speeds from **1 kb/s to 20 kb/s**, DLIN ensures seamless transmission and reception of LIN messages compliant with:

- **LIN 1.3**
- **LIN 2.1**

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- **LIN 2.2A**

DLIN acts as a **bridge to APB, AHB, and AXI bus interfaces**, providing a versatile softcore solution for both **FPGA and ASIC** implementations. Its compact, cost-effective design makes it ideal for **intelligent sensors, actuators, and automotive nodes**, where full CAN bandwidth is unnecessary.

FLEXIBLE MASTER AND SLAVE OPERATION

The DLIN IP Core can operate as either a **master or slave node**, with work modes determined by the connected **microprocessor or microcontroller**. The core continuously reports the **status of transfers** and detects a wide range of **LIN error conditions**, including:

- Overrun
- Framing
- Parity
- Timeout

A **programmable timer** further enhances reliability by detecting synchronization and timeout errors, ensuring robust communication across automotive networks.

SAFETY-ENHANCED DESIGN WITH ISO 26262 COMPLIANCE

The DLIN IP Core is offered in **two versions**:

- **Basic Version** — optimized for standard LIN applications
- **Safety-Enhanced Version** — developed as an **ISO 26262-10 Safety Element out of Context (SEooC)**

The Safety-Enhanced variant includes optional **functional safety mechanisms** and comes with comprehensive **ISO 26262 soft IP SEooC documentation**, including:

- Full **FMEDA (Failure Modes, Effects, and Diagnostic Analysis)**
- Step-by-step integration instructions
- System-level safety analysis guidance
- Verification through **independent third-party audits**

ASIL-B READY FOR AUTOMOTIVE SAFETY SYSTEMS

Safety metrics confirm compliance with **Automotive Safety Integrity Level ASIL-B**:

- **SPFM > 90%** (Single Point Fault Metric)
- **LFM > 60%** (Latent Fault Metric)

This makes the DLIN IP Core suitable for integration into **ASIL-B automotive safety systems**, with optional availability for **higher ASIL-level designs** upon request.

WHY CHOOSE DCD-SEMI DLIN IP CORE

- Supports **LIN 1.3, 2.1, and 2.2A** standards
- UART half-duplex enhanced, 1–20 kb/s transmission
- Works as **master or slave node**
- Bridges APB, AHB, and AXI bus interfaces
- **FPGA & ASIC ready**
- Safety-Enhanced version with **ISO 26262 SEooC compliance**
- ASIL-B ready with full FMEDA and third-party audited documentation

LIN FuSa white papers

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For technical specifications, integration support, or safety-enhanced options, contact

info@dcd-semi.com

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DCD-SEMI automotive IP Cores

	DCAN	DCAN-FD	DCAN-FD Full	DCAN-XL	DLIN	DSENT	DPSI5
Supported protocol	CAN	CAN-FD	CAN-FD	CAN-XL	LIN	SENT	PSI5
Data rate up to	1Mbps	8Mbps	8Mbps	20Mbps	20kbps	30kbps	189kbps
Cost vs complexity	middle	middle	middle high	high	low	low	middle
Best for	Vehicle networks and industrial automation	High speed communication	DCAN FD + multiple TX/RX buffers/FIFOs, timestamps, advanced message filtering	High-performance automotive	Low-cost automotive nodes	Sensor → ECU timing-based data	Safety sensors (airbag, ABS)
ISO26262 Functional Safety	yes	yes	yes	yes	yes	yes	yes

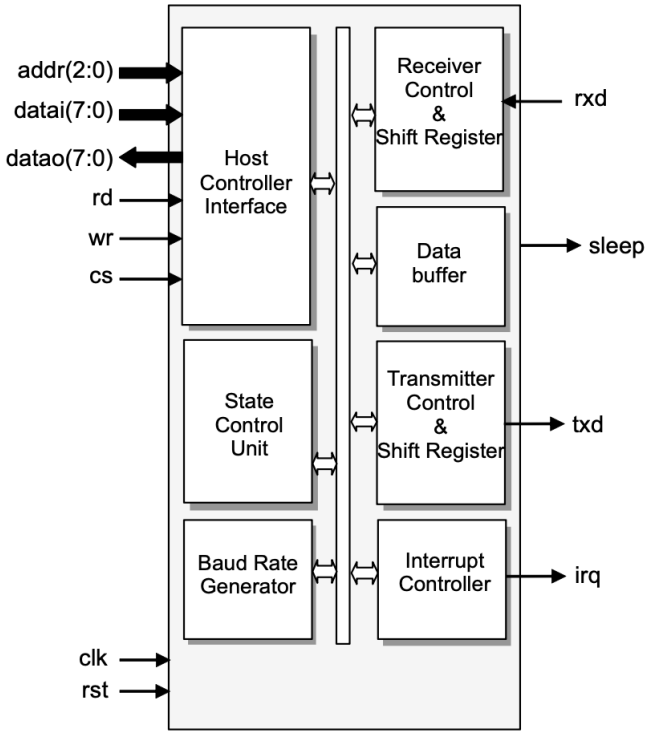
KEY FEATURES

- Conforms with LIN 1.3, LIN 2.1 and LIN 2.2A specification
- UART half-duplex functionality (available only in basic version)
- Automatic LIN Header handling
- Automatic Re-synchronization
- Data rate between 1Kbit/s and 20 Kbit/s
- Master and Slave work mode
- Time-out detection
- Extended error detection
- “Break-in-data” support

UNITS SUMMARY

Host Controller Interface – Accepts inputs from the system bus and generates control signals for other DLIN functional blocks. Address bus ADDR(2:0), selects one of register to be read from/written into. Active level of RD, WR and CS, can be configurable. RD and WR are ignored, unless the DLIN has been selected, by activating CS input. **Control State Unit** – Composed of two state machines, the master and the slave, which control master and slave tasks. The master task handles all bus communication. It must initiate any slave response, by sending out a synch break, a synch field and protected identifier field. Slave task is responsible for sending the response message, if it is addressed by the master. **Baud Rate Generator** – The DLIN contains a programmable 15 bit baud generator, which divides clock input, by a divisor in the range between 1 and (2^{15}-1). The output frequency of the baud generator is 32 x the baud rate. Two registers, called divisor latches DLL and DLH, store the divisor in the 15-bit binary format. **Receiver Control & Shift Register** – Responsible for receiving frame from LIN bus. Provides necessary function for data reception, frame timing and error checking. **Data Buffer** – stores the receive or transmit data. **Transmitter Control & Shift Register** – Performs transmit management function, sends data by LIN bus. **Interrupt Controller** – Works with transmitter, receiver and control unit, to indicate DLIN transmission events or errors. User can configure, which events may generates interrupt by enabled or disabled corresponding bits, in Interrupt Enable register. When interrupt is generated, host can find information about reason by reading LIN Status Register.

SYMBOL



PERFORMANCE

The following table gives a survey about the Core area and performance in **XILINX FPGA** devices after Place & Route (all key features included):

Device	Speed grade	LUT/Slice	F_{max}
ZYNQ-7000	-3	620	263
ZYNQ	-3	521/228	270
KINTEX Ultra Scale	-3	516	330
KINTEX 7	-3	624	294
ARTIX 7	-3	495/184	308
VIRTEX Ultra Scale	-3	539	330
VIRTEX 7	-2	521/159	416
VIRTEX 6	-2	496/178	282
VIRTEX 5	-2	455/190	299
VIRTEX 4	-12	606/416	202
SPARTAN 6	-3	511/167	127
SPARTAN 3E	-5	574/412	124
SPARTAN 3	-5	604/415	121

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

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APPLICATIONS

- Automotive, industrial
- Embedded communication systems

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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