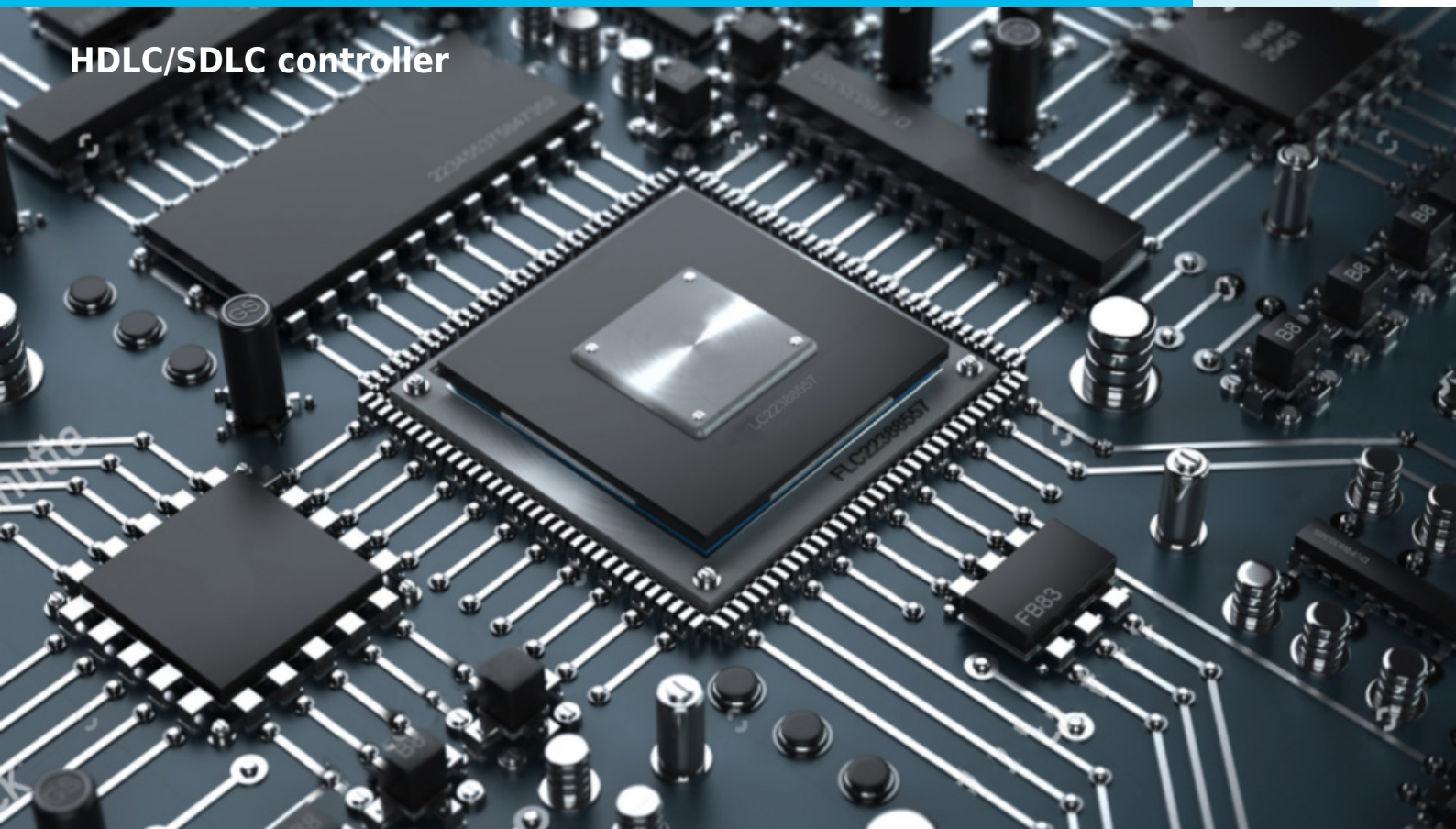


DHDLC



HDLC/SDLC controller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DHDLC bridge to APB, AHB, and AXI bus, provides versatile support for a widely used HDLC transmission protocol. It manages the **bit stuffing process**, both **address appending** and **detection**. And if it's not enough, let's just mention that DCD's IP Core **supports CRC16** and **CRC32** computation. **Increased system performance and reduced CPU overload** are a must-be, thanks to the presence of separate receiver and transmitter FIFO buffers, maskable interrupt, and DMA interface requests. The **DHDLC is a fully scalable** IP Core, which makes it a perfect solution for both high-end and deeply embedded projects. It's tailored to your project needs and can be **provided with:**

- small 8-bit SRAM-like interface
- 32-bit full AXI4 slave interface with burst support
- AXI4Lite interface
- AHB and APB slave interfaces

The optional **Frame Status Buffer** stores information about frame size and error conditions. Moreover, the size of the receiver and transmitter FIFO buffers is configurable. You can also **easily remove unused features before the synthesis** process. All that and much more make the DHDLC an ideal solution for very popular higher-level protocol implementations like e.g. **PPP (Point-to-Point), X.25, V.42, LAB-B, SDLC, ISDN**, and many others.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- **Altera / Intel,**
- **Xilinx / AMD,**
- **Lattice,**
- **Microsemi / Microchip,**
and others.
- **TSMC**
- **UMC**
- **SK Hynix**
and others.

KEY FEATURES

- Two separate receiver and transmitter interfaces.
- Two separate, configurable FIFO buffers for receiver and transmitter
- Bit stuffing and unstuffing
- Address recognition for receiver and address insertion for transmitter
- Two or one byte address field
- CRC-16 and CRC-32 computation and checking
- Collision detection
- Byte alignment error detection
- Programmable number of bits for idle detection
- NRZI coding support
- Shared flags, shared zeroes support
- Pad fill with flags option
- Transmitter clock generation
- 8-bit, 16-bit, 32-bit CPU interface
- Interrupt output for handling control flags and FIFOs' filling
- Configurable core parameters
- **Available system interface wrappers:**
 - **AMBA - APB / AHB / AXI Bus**
 - **Altera Avalon Bus**
 - **Xilinx OPB Bus**

UNITS SUMMARY

CPU Interface - it performs operations of reading and writing internal registers of module.

Serial Interface - it performs bit stuffing and unstuffing, NRZI coding, collision detection, CRC calculation, flags and abort detection, idle detection and synchronizes serial inputs with main clock domain.

FIFO control - it manages access to FIFO buffers of receive and transmitter.

Control Unit - it controls HDLC frame and services request from CPU interface module.

Clock Divider - it generates divided clock signal for TXCLKO output.

DESIGN FEATURES

The DHDLC IP core is fully synchronous, with one clock domain design. All parameters are configurable by a CPU. There is also capability for setting parameters by modification of constants in the source file. There is no need to waste silicon resources on unused features and constant settings.

APPLICATIONS

- CPU based applications with serial interface based on HDLC/SDLC protocol
- Telecommunication

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** devices, after Place & Route (all key features included):

Device	Speed grade	Area [gates]	F _{max} [MHz]
0.18u speed	typical	2 900	350
0.18u area	typical	2 700	100
0.25u speed	typical	2 900	280
0.25u area	typical	2 700	100

DELIVERABLES

- **Source code:**
 - VERILOG or VHDL Source Code
 - VERILOG or VHDL test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
 - Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
 - Synthesis scripts
 - Example application
- **Netlist**
 - Netlist for selected FPGA family
 - Sample FPGA project
 - Technical documentation
 - HDL core specification
 - Datasheet
- **Technical support**
 - IP Core implementation
 - 12 months maintenance
 - Delivery of the IP Core and documentation updates
 - Phone & email support

- Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

- **Single-Site license option** - dedicated to small and middle sized companies which run their business at one place.

- **Multi-Site license option** - dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:

- VHDL or Verilog RTL synthesizable source code (called HDL Source code)

- FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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