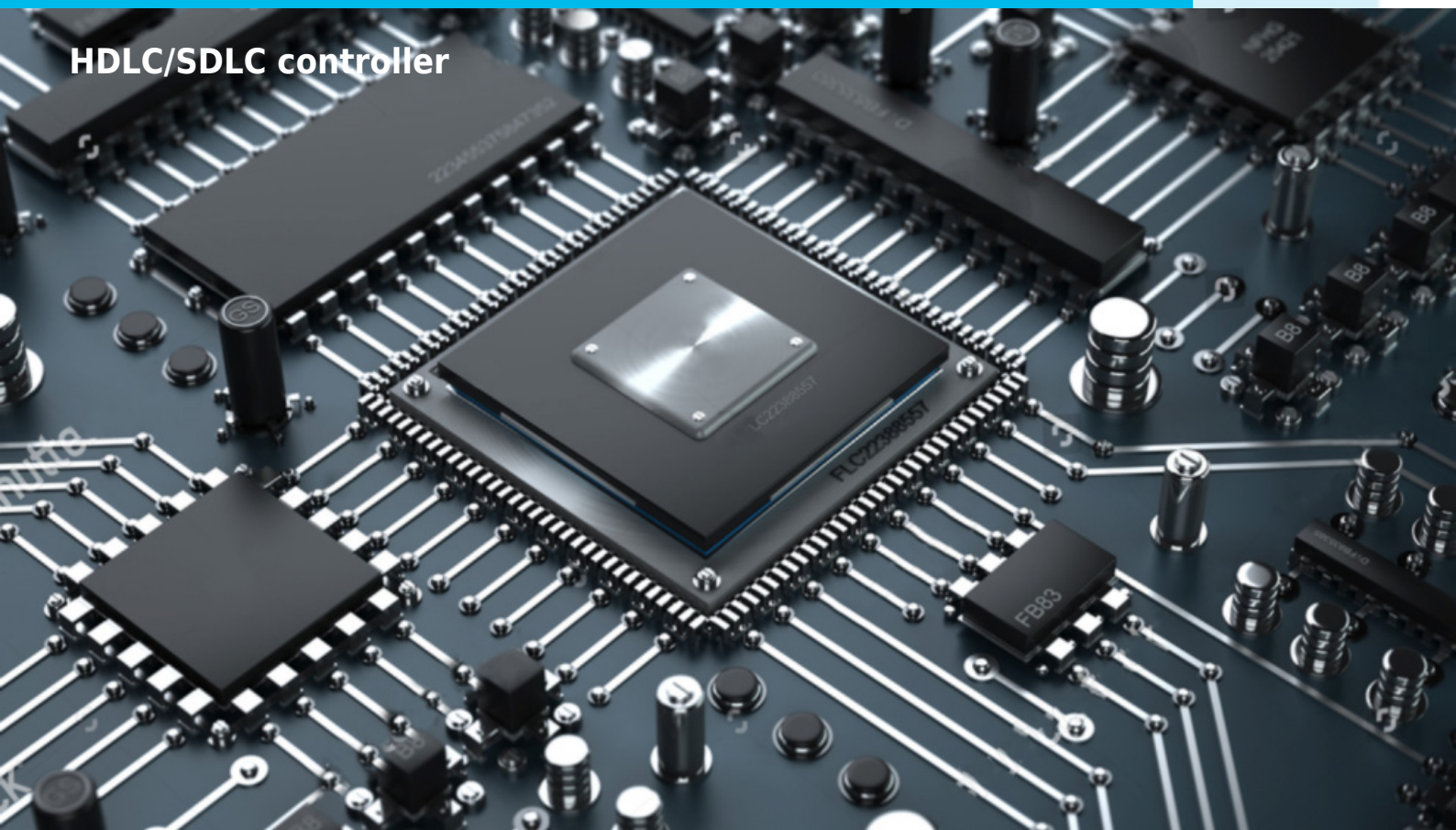
DIGITAL CORE DESIGN

DHDLC

HDLC/SDLC controller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DHDLC IP CORE – HDLC PROTOCOL CONTROLLER WITH AXI, AHB, AND APB INTERFACES

The **DHDLC IP Core** from **DCD-SEMI** is a high-performance **HDLC protocol controller** designed for seamless integration into **FPGA and ASIC designs**. Acting as a flexible **HDLC bridge to APB, AHB, and AXI bus architectures**, DHDLC enables reliable implementation of one of the most widely used serial communication protocols in embedded and networking systems.

The core fully offloads **HDLC frame handling** from the CPU, including **bit stuffing and unstuffing**, **address field insertion and detection**, and **frame integrity verification** using **CRC16 and CRC32**. This significantly reduces processor load while increasing overall system throughput and determinism.

Key Features for FPGA and ASIC Designs

- **Complete HDLC protocol support** with transmit and receive paths
- **CRC16 and CRC32 generation and checking**
- **Independent TX and RX FIFO buffers** to maximize data throughput
- **Maskable interrupt system and DMA request support** for low-latency data handling
- **Optional Frame Status Buffer** reporting frame length and error conditions
- **Configurable FIFO depths** for optimal resource utilization
- **Synthesis-time feature trimming** to reduce area and power consumption

Scalable Bus Interfaces

The DHDLC IP Core is fully scalable and tailored to project-specific requirements, making it suitable for both **deeply embedded systems** and **high-end SoCs**. Supported host interfaces include:

- **Compact 8-bit SRAM-like interface**
- **32-bit AXI4 slave interface with burst support**
- **AXI4-Lite interface**
- **AHB and APB slave interfaces**

This flexibility allows easy integration into modern SoC architectures and legacy designs alike.

Optimized for System Performance

By combining hardware-based protocol processing with **FIFO buffering, DMA support, and interrupt handling**, the DHDLC IP Core ensures **high data throughput**, **predictable latency**, and **minimal CPU intervention**—critical requirements for real-time and communication-intensive applications.

Target Applications

The DHDLC IP Core is an ideal building block for implementing higher-level protocols and communication stacks, including:

- **PPP (Point-to-Point Protocol)**
- **X.25**
- **V.42**
- **LAP-B**
- **SDLC**
- **ISDN**
- and many other HDLC-based protocols

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Why Choose DCD-SEMI DHDLC IP Core?

- Proven **FPGA- and ASIC-ready IP**
- Highly **configurable and scalable architecture**
- Reduced integration effort and faster time-to-market
- Optimized for **performance, area efficiency, and power**

The **DHDLC IP Core** delivers a robust, configurable, and production-ready HDLC solution for engineers designing modern communication-enabled systems.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Two separate receiver and transmitter interfaces.
- Two separate, configurable FIFO buffers for receiver and transmitter
- Bit stuffing and unstuffing
- Address recognition for receiver and address insertion for transmitter
- Two or one byte address field
- CRC-16 and CRC-32 computation and checking
- Collision detection
- Byte alignment error detection
- Programmable number of bits for idle detection
- NRZI coding support
- Shared flags, shared zeroes support
- Pad fill with flags option
- Transmitter clock generation
- 8-bit, 16-bit, 32-bit CPU interface
- Interrupt output for handling control flags and FIFOs' filling
- Configurable core parameters

UNITS SUMMARY

CPU Interface – it performs operations of reading and writing internal registers of module.
Serial Interface – it performs bit stuffing and unstuffing, NRZI coding, collision detection, CRC calculation, flags and abort detection, idle detection and synchronizes serial inputs with main clock domain.
FIFO control – it manages access to FIFO buffers of receive and transmitter.
Control Unit – it controls HDLC frame and services request from CPU interface module.
Clock Divider – it generates divided clock signal for TXCLKO output.

DESIGN FEATURES

The DHDLC IP core is fully synchronous, with one clock domain design. All parameters are configurable by a CPU. There is also capability for setting parameters by modification of constants in the source file. There is no need to waste silicon resources on unused features and constant settings.

APPLICATIONS

- CPU based applications with serial interface based on HDLC/SDLC protocol
- Telecommunication

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** devices, after Place & Route (all key features included):

Device	Speed grade	Area [gates]	F_{max} [MHz]
0.18u speed	typical	2 900	350
0.18u area	typical	2 700	100
0.25u speed	typical	2 900	280
0.25u area	typical	2 700	100

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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