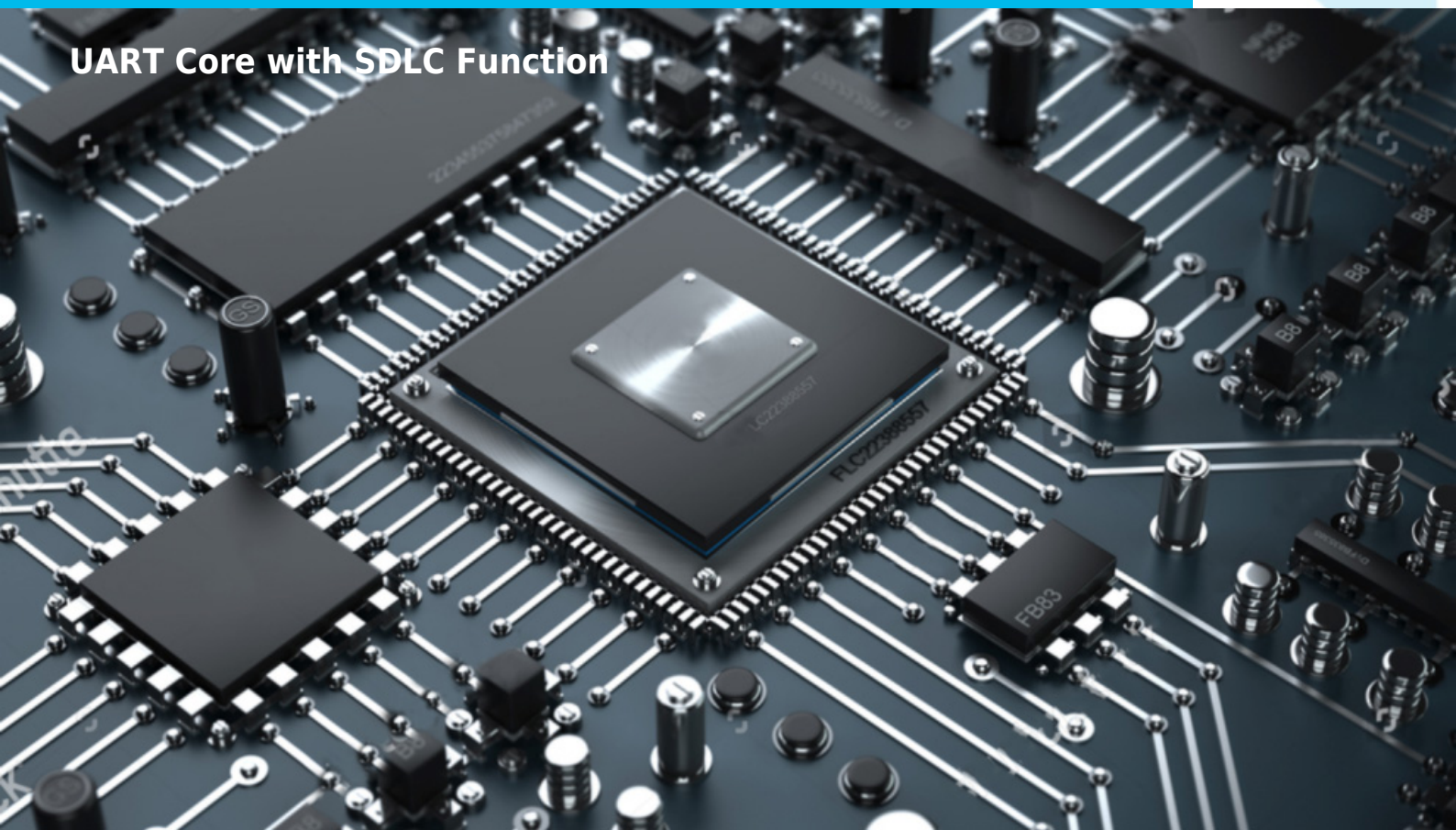
DIGITAL CORE DESIGN

D8530

UART Core with SDLC Function



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D8530 IP Core – Dual-Channel USART Controller for FPGA & ASIC

The **D8530 IP Core** from **DCD-SEMI** is a highly versatile **dual-channel USART (Universal Synchronous/Asynchronous Receiver/Transmitter)** designed for seamless integration into **FPGA and ASIC designs**. Acting as a configurable **bridge to APB, AHB, and AXI bus architectures**, the D8530 enables reliable serial communication across a wide range of embedded, industrial, and telecommunications systems.

Designed for use with **8-bit and 16-bit microprocessors**, the D8530 operates as a **serial-to-parallel and parallel-to-serial controller**, offering exceptional flexibility through software configurability. Integrated **on-chip baud rate generators** allow precise timing control without external components, reducing system complexity.

Comprehensive Serial Protocol Support

The D8530 IP Core supports virtually all serial communication formats, including:

- **Asynchronous UART modes**
- **Synchronous byte-oriented protocols** (e.g. **IBM® Bisync**)
- **Synchronous bit-oriented protocols**, such as **HDLC** and **IBM SDLC**

In synchronous modes, the core can **generate and check CRC codes**, enabling robust data integrity verification across multiple protocol variants.

Advanced Configuration and Control

Each channel of the D8530 is controlled via a rich register set, consisting of **14 write registers and 7 read registers per channel** (depending on configuration). Within each operating mode, the core supports extensive protocol customization, including:

- Odd or even **parity checking**
- **Variable data sizes**, stop bits, and framing formats
- **Character insertion and deletion**
- **Break and abort generation and detection**
- Programmable **CRC generation and checking**

This level of configurability makes the D8530 suitable for both **legacy communication standards** and modern embedded designs.

Modem Control and GPIO Flexibility

The D8530 provides **full modem control on both channels**, enabling seamless integration with traditional communication hardware. In applications where modem signaling is not required, these signals can be repurposed as **general-purpose I/O**, further increasing design flexibility.

Scalable Bus Interfaces

To fit a wide range of SoC architectures, the D8530 IP Core can be delivered with:

- **AXI4 or AXI4-Lite slave interface**
- **AHB slave interface**
- **APB slave interface**

This scalability makes the D8530 an ideal solution for both **deeply embedded systems** and **high-performance FPGA-based platforms**.

Typical Applications

- Telecommunications equipment
- Industrial controllers
- LAN and networking devices
- Legacy protocol bridging
- FPGA-based SoCs requiring flexible serial interfaces

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ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Software compatible with Z85C30
- Dual Channel: A, B
- Configuration capability
- Asynchronous mode:
  - Asynchronous (x16, x32, or x64 clock
  - Isochronous (x1 clock)
- Character-Oriented mode:
  - Monosynchronous
  - Bisynchronous
  - External Synchronous
- Bit-Oriented mode:
  - SDLC/HDLC
  - SDLC/HDLC Loop
- Complete status reporting capabilities
- Receiver data FIFO and Error FIFO
- SDLC Frame FIFO
- Data encoder\decoder:
  - NRZ, NRZI
  - FM0, FM1
  - Manchester (require external logic)
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Auto Echo
  - Break, parity, overrun, framing error simulation
- Fully synchronous design with no internal tristate buffers

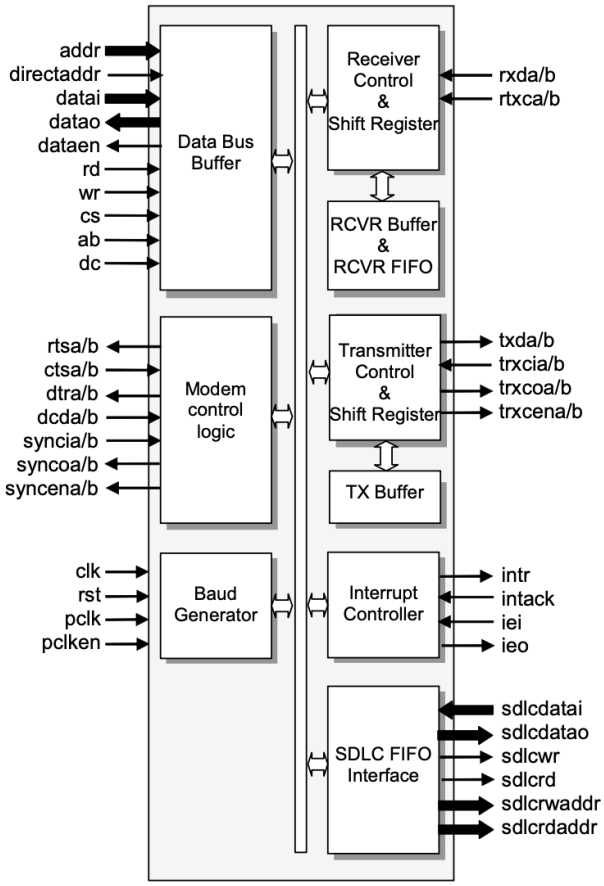
Transmission modes:

- Synchronous Byte (Bisync) features
  - *5 to 8 Bit characters*
  - *Programmable Sync character*
  - *Transparent text mode operation*
  - *Automatic Sync insertion during Idle*
  - *Hardware CRC generation and detection*
  - *CRC-16 or CRC-CCITT polynomials*
- Asynchronous Features
  - *5-8 Bits per character*
  - *1, 1,5 and 2 stop bits*
  - *Break generation and detection*
  - *Parity, overrun and framing error detection*
  - *Even, Odd or no parity*
- Modem controls and indicators
  - *CTS, DSR, DCD and RI lines, usable for modem control or user defined input*
  - *DTR and RTS usable for modem control or user defined output*
- Synchronous SDLC features
  - *1-8 Bits character (transmitter)*
  - *5-8 Bits receiver character*
  - *Hardware address recognition*
  - *Automatic zero insertion and deletion*
  - *I-Field residue handling*
  - *Automatic flag insertion between messages*
  - *Hardware CRC generation and reception*
- Interrupt system features
  - Channel functions and timers internally prioritized
  - Channel functions and timers generate unique interrupt mode
  - Prioritized Daisy-chain
- LOOPBACK test mode

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

BLOCK DIAGRAM



PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA** devices after Place & Route:

Device	LE/ALM	Memory Bits	F_{max}
ARIA V	1 966/1 052	608	118 MHz
CYCLONE	2 730	608	68 MHz
CYCLONE II	2 883	608	90 MHz
CYCLONE III	2 896	608	109 MHz
CYCLONE IV E	2 869	608	112 MHz

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CYCLONE IV 6X	2 881	608	112 MHz
CYCLONE V	1 967	608	89 MHz
STRATIX	2 730	608	72 MHz
STRATIX II	2 037	608	123 MHz
STRATIX III	1 962/997	608	214 MHz
STRATIX IV	1 952/997	608	196 MHz
STRATIX V	1 950/1 044	608	219 MHz
MAX 10	2 935	608	90 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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