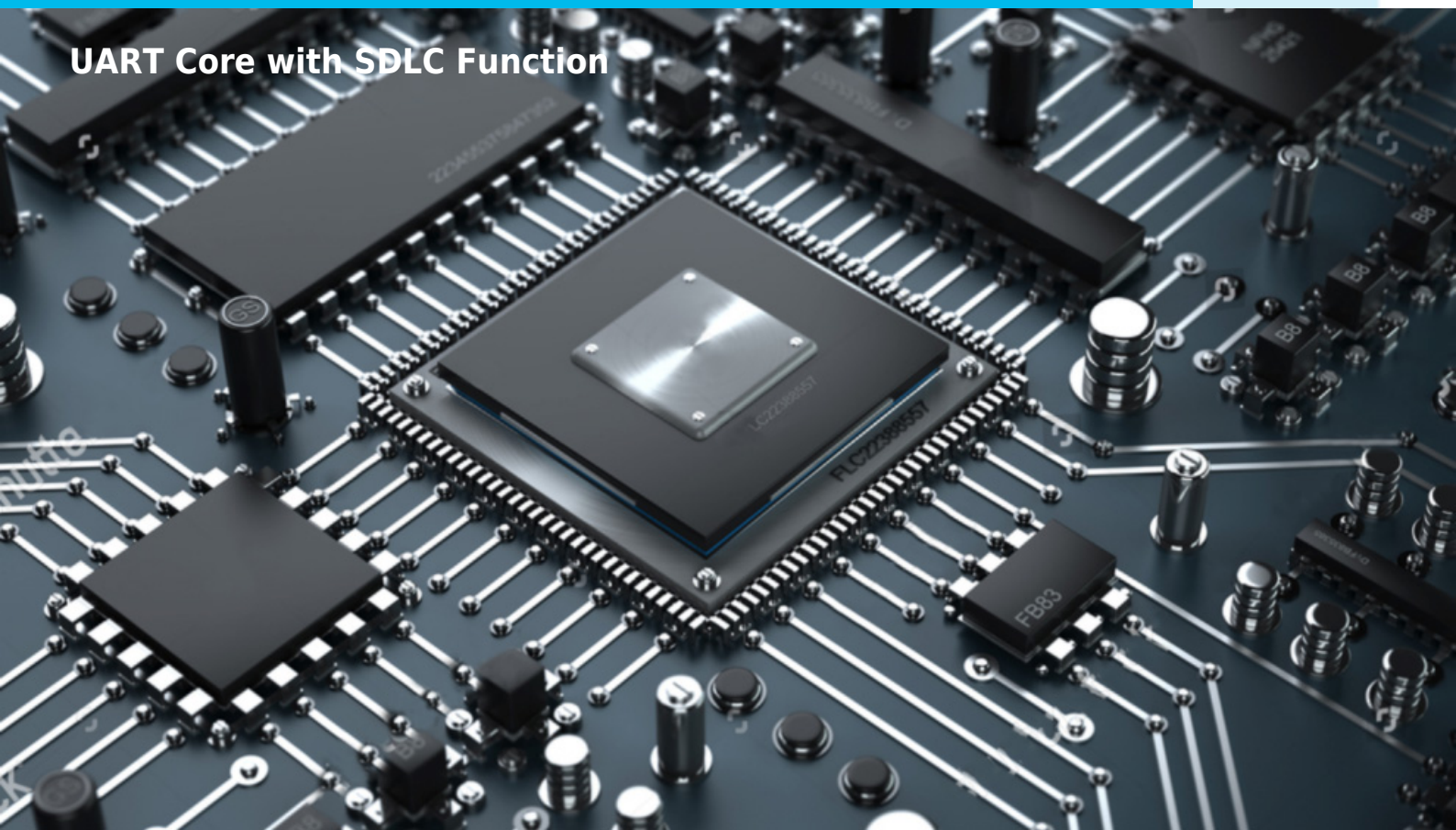
DIGITAL CORE DESIGN

D85C30

UART Core with SDLC Function



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D8530 bridge to APB, AHB, AXI bus, it is a dual channel USART (Universal Synchronous/Asynchronous Receiver/Transmitter) device, designed for use with 8 and 16-bit microprocessors. It works as **serial-to-parallel**, **parallel-to-serial converter/controller** and can be software-configured to satisfy wide range of serial communications applications. The device contains variety of new, sophisticated internal functions, including on-chip baud rate generators. The D85C30 handles asynchronous formats, synchronous byte-oriented protocols (such as **IBM® Bisync)** and synchronous bit-oriented protocols, like HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.). It can also can **generate and check CRC codes** in any synchronous mode and can be programmed to check data integrity in various modes. The D85C30 supports modem control in both channels – in applications where these controls are not needed, modem controls can be used for general-purpose I/O. You can configure the IP Core to handle all synchronous formats, regardless of data size, number of stop bits or parity requirements. The D85C30 is controlled through access to 14 Write registers and 7 Read registers per channel (the number of the registers varies depending on the version). Within each operating mode the D85C30 allows **protocol variations** by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

KEY FEATURES

- Software compatible with Z85C30
- Dual Channel: A, B
- Configuration capability
- Asynchronous mode:
  - Asynchronous (x16, x32, or x64 clock
  - Isochronous (x1 clock)
- Character-Oriented mode:
  - Monosynchronous
  - Bisynchronous
  - External Synchronous
- Bit-Oriented mode:
  - SDLC/HDLC
  - SDLC/HDLC Loop
- Complete status reporting capabilities
- Receiver data FIFO and Error FIFO
- SDLC Frame FIFO
- Data encoder\decoder:
  - NRZ, NRZI
  - FM0, FM1
  - Manchester (require external logic)
- Line break generation and detection
- Internal diagnostic capabilities:
  - Loop-back controls for communications link fault isolation
  - Auto Echo
  - Break, parity, overrun, framing error simulation
- Fully synchronous design with no internal tristate buffers

Transmission modes:

- Synchronous Byte (Bisync) features
  - *5 to 8 Bit characters*
  - *Programmable Sync character*
  - *Transparent text mode operation*
  - *Automatic Sync insertion during Idle*
  - *Hardware CRC generation and detection*
  - *CRC-16 or CRC-CCITT polynomials*
- Asynchronous Features
  - *5-8 Bits per character*
  - *1, 1,5 and 2 stop bits*
  - *Break generation and detection*
  - *Parity, overrun and framing error detection*
  - *Even, Odd or no parity*
- Modem controls and indicators
  - *CTS, DSR, DCD and RI lines, usable for modem control or user defined input*
  - *DTR and RTS usable for modem control or user defined output*
- Synchronous SDLC features
  - *1-8 Bits character (transmitter)*
  - *5-8 Bits receiver character*
  - *Hardware address recognition*
  - *Automatic zero insertion and deletion*
  - *I-Field residue handling*
  - *Automatic flag insertion between messages*
  - *Hardware CRC generation and reception*
- Interrupt system features
  - Channel functions and timers internally prioritized
  - Channel functions and timers generate unique interrupt mode
  - Prioritized Daisy-chain
- LOOPBACK test mode
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

APPLICATIONS

- Serial Data communications applications
- Modem interface
- Embedded microprocessor boards

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	LE/ALM	Memory Bits	F_{max}
ARIA	2 033/943	608	83 MHz
ARIA II	1 954/943	608	167 MHz
ARIA V	1 966/1 052	608	118 MHz
CYCLONE	2 730	608	68 MHz
CYCLONE II	2 883	608	90 MHz
CYCLONE III	2 896	608	109 MHz
CYCLONE IV E	2 869	608	112 MHz
CYCLONE IV 6X	2 881	608	112 MHz
CYCLONE V	1 967	608	89 MHz
STRATIX	2 730	608	72 MHz
STRATIX II	2 037	608	123 MHz
STRATIX III	1 962/997	608	214 MHz
STRATIX IV	1 952/997	608	196 MHz
STRATIX V	1 950/1 044	608	219 MHz
MAX 10	2 935	608	90 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

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