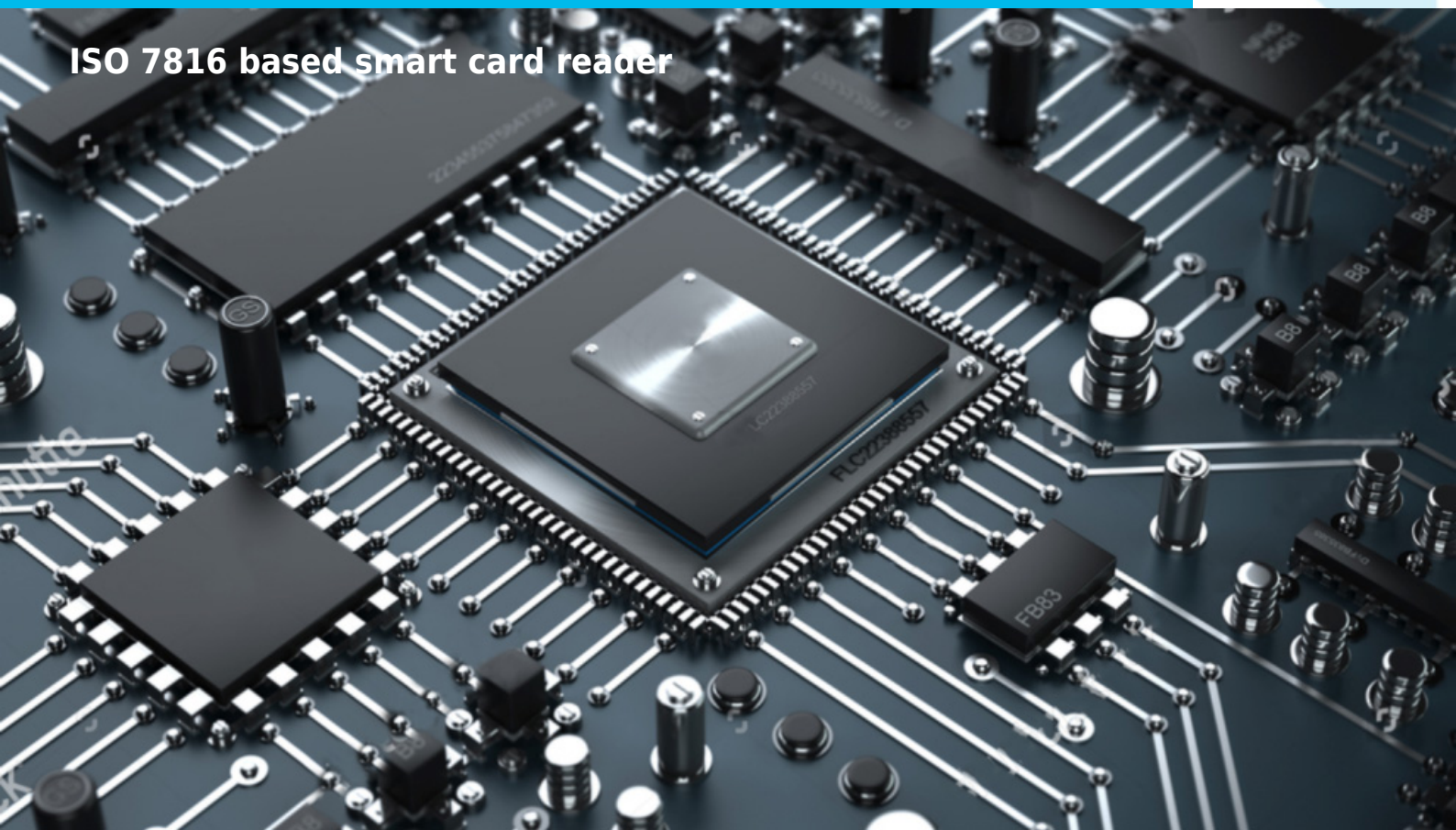
DIGITAL CORE DESIGN

DSMART

ISO 7816 based smart card reader



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DSMART bridge to APB, AHB, and AXI bus, is a fast, versatile, and cost-competitive core intended for smart card reader applications. It provides a communication interface with a smart card based on **ISO 7816-3/EMV4.2/4.3** requirements. DCD's IP Core implements hardware support for both T0 character-oriented protocol and T1 block-oriented protocol. It was designed to combine **highly reduced CPU utilization and low area consumption.** The DSMART is able to **activate and deactivate cards, perform resets, handle ATR reception, and offers many additional features**. Configuration options allow you to adjust the DSMART to your particular needs and choose proprietary options, which will be the most suitable for the design. Data transfer to and from the host system can be interrupt-driven or executed through Direct Memory Access (DMA). The automatic convention detection and decoding mechanism ensures the **exact result** regardless of the used convention. Elementary Time Unit (ETU) – time duration of one bit is decoded from the received ATR interface byte and generated automatically. The card clock divider provides a non-gated clock with a wide range of possible frequencies. A **special power down mode** was implemented in which the card clock is being held in two possible states, depending on the card parameter. Error signaling and character repetition are automatic for the T0 protocol. The DSMART also incorporates optional **CRC/LRC hardware checking and generation mechanism**, which gives a convention-independent result. The received CRC/LRC is not stored in the FIFO but can be read in case of CRC/LRC error. Additionally, the optional block length counter provides security of the DMA block transfer and automatic CRC/LRC, subjoining with a manual affixing option. A special block mode handles block transfer automatically. Status and error registers provide necessary information about the FIFO state, errors, and card events.

* Note that DSMART works with all major CPUs and is 100% compatible with DCD's MCUs – enabling the same – cryptography.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- Compatible with the ISO 7816-3: 2006 and EMV 4.2/4.3 standard
- Support for asynchronous Smart Cards
- Dual configurable length FIFO with two programmable thresholds
- Card detection input
- Software-configurable interrupts
- Automatic convention detection and decoding
- Programmable non-gated card clock generator
- Automatic ETU generator
- DMA support for transmit and receive
- Hardware CRC and LRC calculations
- Card power down mode with clock stop high and clock stop low possibility
- Special fast block mode for T1 protocol (optional)
- CRC/LRC hardware generation and checking
- Byte counter with automatic CRC/LRC affixing (optional)
- No tri-state buffers
- Fully synchronous synthesizable design
- **Available system interface wrappers:**
  - **AMBA – APB / AHB / AXI Bus**
  - **Altera Avalon Bus**
  - **Xilinx OPB Bus**

UNITS SUMMARY

Interface – Responsible for communication with the CPU unit. Contains registers which inform about the status and control the DSMART actions. Access to the registers is through the address strobe (ADDR[4:0]) and the data strobe (DATAI[7:0], DATAO[7:0]). To control the read and write process the write (wr) and read (rd) pins are used. Both are active high. The active low Chip Select (CS) signal is used to enable or disable data interface.

RX_FIFO (Receiver FIFO) – The FIFO depth is configurable. It has four trigger levels which can be the source of the interrupt or DMA requests. The receiver FIFO will continue to store bytes, until it is full and will not accept any more bytes. The DSMART has protection system which prevents from unwanted random read.

TX_FIFO (Transmitter FIFO) – The FIFO depth is configurable. It has four trigger levels which can be the source of the interrupt or DMA requests. The Transmitter FIFO will continue to send bytes until it is empty. The DSMART has protection system which prevents from unwanted random write.

ISO 7816-3 UART – In general it is responsible for transmitting and receiving data according to the ISO standard. It automatically generates appropriate transmission clock (ETU) and preserve all timing requirements.

CARD_CONTROL MODULE – This module manages activation, deactivation, reset and clock stop. All timing requirements are automatically preserved.
CRC and LRC Hardware Generator (OPTIONAL) – It either checks the CRC\LRC of the incoming bytes or generates and appends it to the message. This process can be fully automated or CPU controlled. The CRC is checked against polynomial and LRC is XOR of all bytes in the message.
Block Module (OPTIONAL) – Special improvement for block oriented T1 protocol. It allows managing the block transfer much more effectively with smaller CPU resources consumption. This solution will give effects using the Direct Memory Access and CRC/LRC Hardware Generator.
DMA module – The direct memory access module allows transferring data to and from target memory without the CPU intervention. Both acknowledge and request signals are active high.

APPLICATIONS

- General purpose smart card readers
- SO-7816 / EMV Bridges
- Personal Wireless devices & SIM Readers in Telecom
- Payphones and vending machines
- Personal identification
- Satellite TV security
- Health care records storage

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route of exemplary devices:

Device	LE/ALM	Memory Bits	F_{max}
Aria GX	542	256	147 MHz
Aria 5	394/290	256	366 Mhz
Cyclone	784	256	130 Mhz
Cyclone 2	783	256	152 MHz
Cyclone 3	775	256	173Mhz
Cyclone 4	778	256	152 Mhz
Cyclone 5	362	256	151 Mhz
Stratix	771	256	151 Mhz
Stratix 2	534/282	256	234 Mhz
Stratix 3	532/330	256	349 Mhz
Stratix 4	533/330	256	352 MHz
Stratix 5	542/330	256	308Mhz
Stratix GX	771	256	140 Mhz
Stratix 2 GX	534/282	256	236 Mhz

Maximal setting with included block mode, CRC/LRC and length counter. FIFO depth is 16 bytes (balanced settings).

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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