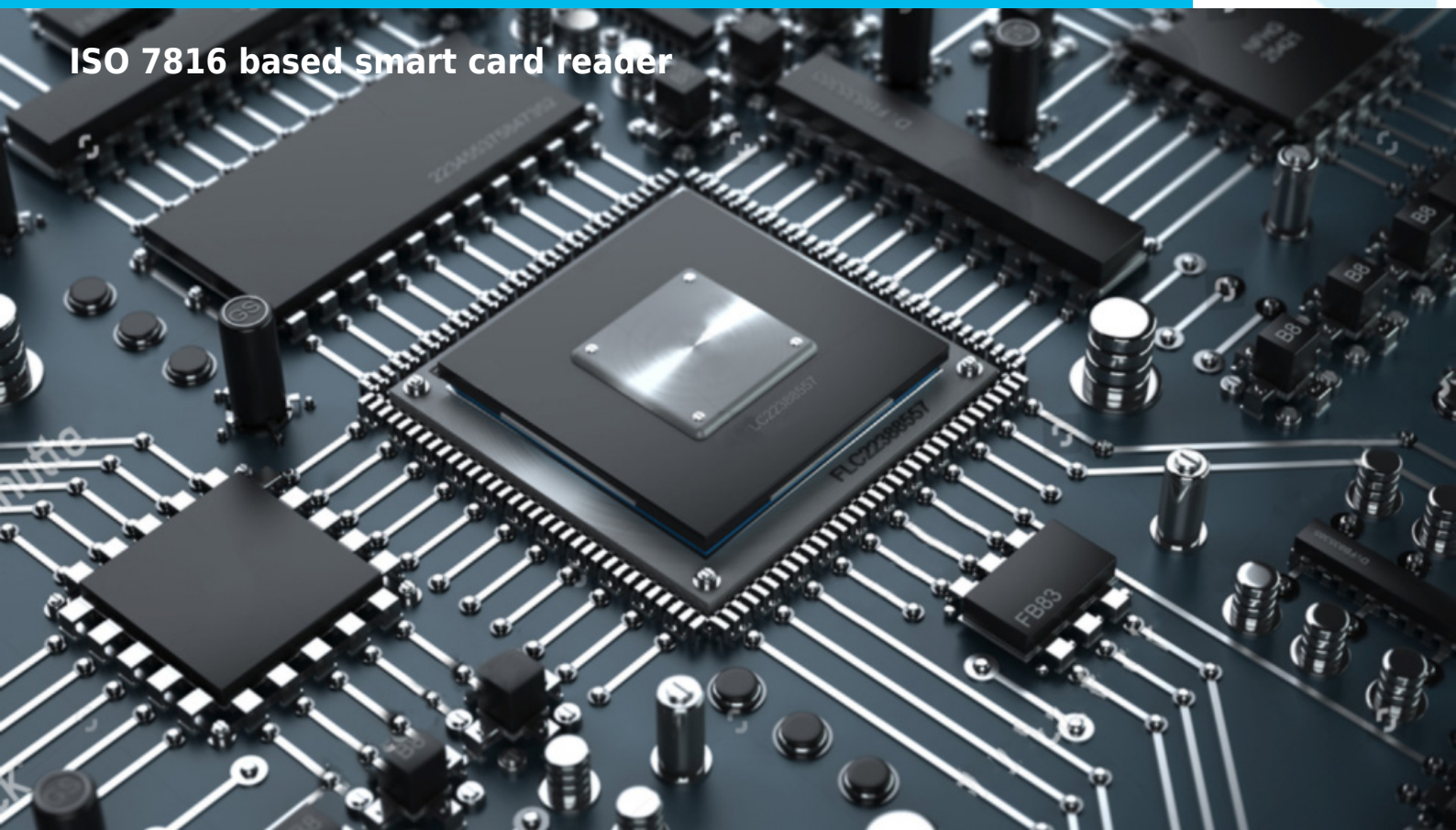
DIGITAL CORE DESIGN

PRIVATE: DSMART



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DSMART IP Core – Smart Card Interface Controller for FPGA & ASIC

The **DSMART IP Core** from **DCD-SEMI** is a fast, versatile, and cost-efficient **smart card reader controller** designed for **FPGA and ASIC implementations**. Acting as a scalable **bridge to APB, AHB, and AXI bus architectures**, DSMART provides a complete hardware interface for smart cards compliant with **ISO 7816-3** and **EMV 4.2 / 4.3** standards.

The core implements full hardware support for both major smart card communication protocols:

- **T=0** – character-oriented protocol
- **T=1** – block-oriented protocol

DSMART is optimized for **low CPU utilization and minimal silicon area**, making it well suited for secure embedded systems and high-volume designs.

Complete Smart Card Lifecycle Management

DSMART handles the full smart card operation sequence in hardware, including:

- Card **activation and deactivation**
- **Cold and warm reset**
- **ATR (Answer To Reset) reception and decoding**
- Automatic **convention detection and decoding**

The automatic convention handling ensures **correct operation regardless of direct or inverse convention**, eliminating software complexity.

Timing, Clocking, and Power Management

The core automatically decodes the **Elementary Time Unit (ETU)** from the ATR interface bytes and generates the correct bit timing internally. A **programmable card clock divider** delivers a non-gated clock with a wide frequency range.

A dedicated **power-down mode** is available, holding the card clock in one of two defined states according to card parameters, enabling low-power operation in secure systems.

High-Performance Data Transfer with DMA Support

Data transfer between the smart card and host system can be performed using:

- **Interrupt-driven operation**
- **Direct Memory Access (DMA)**

Optional hardware features include:

- **CRC/LRC generation and checking** (convention-independent)
- **Block length counter** for secure DMA transfers
- Automatic or manual CRC/LRC handling
- Dedicated **block transfer mode** for T=1 protocol

For T=0 protocol, **error signaling and character repetition** are handled automatically in hardware.

Diagnostics, Status, and Error Reporting

DSMART includes comprehensive **status and error registers** providing real-time information about:

- FIFO state
- Communication errors
- Card insertion, removal, and event status

The received CRC/LRC is not stored in the FIFO but can be read separately in the event of a CRC/LRC error, ensuring clean data handling.

Integration and Compatibility

DSMART is a **technology-independent IP Core** that

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integrates seamlessly into modern SoC designs via:

- **AMBA APB interface**
- **AMBA AHB interface**
- **AMBA AXI interface**

The core works with **all major CPU architectures** and is **100% compatible with DCD's MCUs**, enabling consistent cryptographic and security implementations across platforms.

Typical Applications

- Smart card readers
- Secure identification systems
- Payment terminals (EMV-compliant)
- Access control and authentication devices
- Secure embedded FPGA and ASIC designs

* Note that DSMART works with all major CPUs and is 100% compatible with DCD's MCUs – enabling the same – cryptography.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

KEY FEATURES

- Compatible with the ISO 7816-3: 2006 and EMV 4.2/4.3 standard
- Support for asynchronous Smart Cards
- Dual configurable length FIFO with two programmable thresholds
- Card detection input
- Software-configurable interrupts
- Automatic convention detection and decoding
- Programmable non-gated card clock generator
- Automatic ETU generator
- DMA support for transmit and receive
- Hardware CRC and LRC calculations
- Card power down mode with clock stop high and clock stop low possibility
- Special fast block mode for T1 protocol (optional)
- CRC/LRC hardware generation and checking
- Byte counter with automatic CRC/LRC affixing (optional)
- No tri-state buffers
- Fully synchronous synthesizable design

UNITS SUMMARY

Interface – Responsible for communication with the CPU unit. Contains registers which inform about the status and control the DSMART actions. Access to the registers is through the address strobe (ADDR[4:0]) and the data strobe (DATAI[7:0], DATAO[7:0]). To control the read and write process the write (wr) and read (rd) pins are used. Both are active high. The active low Chip Select (CS) signal is used to enable or disable data interface.
RX_FIFO (Receiver FIFO) – The FIFO depth is configurable. It has four trigger levels which can be the source of the interrupt or DMA requests. The receiver FIFO will continue to store bytes, until it is full and will not accept any more bytes. The DSMART has protection system which prevents from unwanted random read.
TX_FIFO (Transmitter FIFO) – The FIFO depth is configurable. It has four trigger levels which can be the source of the interrupt or DMA requests. The Transmitter FIFO will continue to send bytes until it is empty. The DSMART has protection system which prevents from unwanted random write.
ISO 7816-3 UART – In general it is responsible for transmitting and receiving data according to the ISO standard. It automatically generates appropriate transmission clock (ETU) and preserve all timing requirements.
CARD_CONTROL MODULE – This module manages activation, deactivation, reset and clock stop. All timing requirements are automatically preserved.
CRC and LRC Hardware Generator (OPTIONAL) – It either checks the CRC\LRC of the incoming bytes or generates and appends it to the message. This process can be fully automated or CPU controlled. The CRC is checked against polynomial and LRC is XOR of all bytes in the message.
Block Module (OPTIONAL) – Special improvement for block oriented T1 protocol. It allows managing the block transfer much more effectively with smaller CPU resources consumption. This solution will give effects using the Direct Memory Access and CRC/LRC Hardware Generator.
DMA module – The direct memory access module allows transferring data to and from target memory without the CPU intervention. Both acknowledge and request signals are active high.

APPLICATIONS

- General purpose smart card readers
- SO-7816 / EMV Bridges
- Personal Wireless devices & SIM Readers in Telecom
- Payphones and vending machines
- Personal identification
- Satellite TV security
- Health care records storage

PERFORMANCE

The following table gives a survey about the Core area and performance in **Lattice FPGA** devices after Place & Route of exemplary devices:

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Device	Slices/Luts	Memory Bits	F_{max}
ECP	368/592	256	74 MHz
ECP2	383/597	256	84 Mhz
ECP2M	383/597	256	84 Mhz
ECP3	383/600	256	84 Mhz
XP	368/592	256	52 Mhz
XP2	381/594	256	67 Mhz
SC	406/639	256	131 MHz
SCM	405/638	256	118 Mhz

Maximal setting with included block mode, CRC/LRC and length counter. FIFO depth is 16 bytes.

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

DCD-SEMI Sp. z o.o. Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/

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