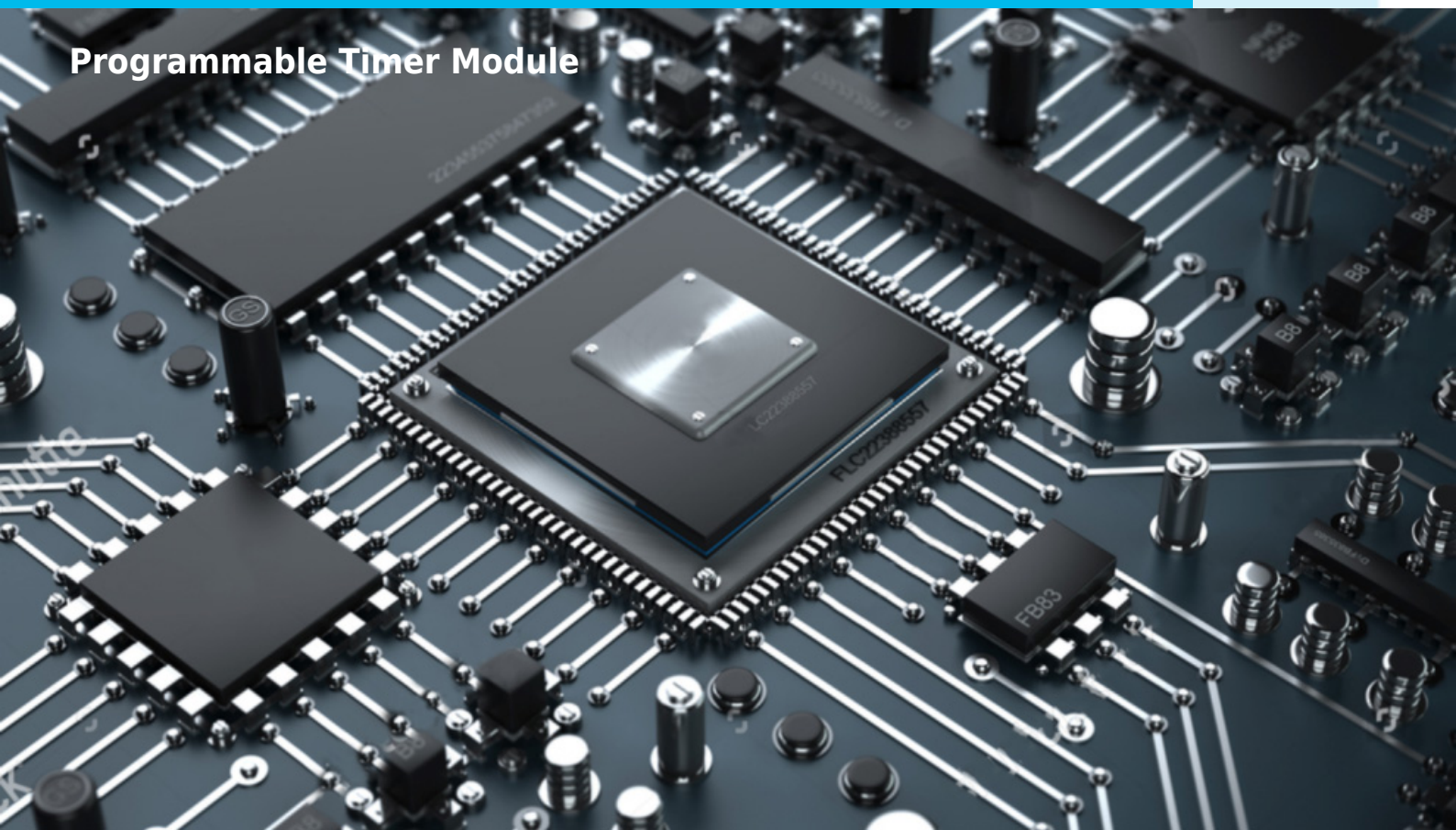
DIGITAL CORE DESIGN

D6840

Programmable Timer Module



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D6840 IP Core — Programmable Timer Module for High-Precision Embedded Applications

Versatile 16-Bit Timer Module for D68xx Processors and Beyond

The **D6840 IP Core** from DCD-SEMI is a **programmable timer module** compatible with the **industry-standard 6840 timer**. Designed for **embedded systems**, the D6840 is ideal for **peripheral devices** in **D68xx processor** architectures, or as a **standalone IP Core** in systems requiring precise timing control.

This timer module features **three independent 16-bit timers**, each with **individual control registers** and **common status registers**, offering flexible timing capabilities for a wide range of applications.

Advanced Timer Functionality

The D6840 supports:

- **Square Wave Generation:** Produce continuous or single-shot waveforms with **adjustable duty cycles**
- **Frequency and Pulse Width Measurement:** Accurate timing and pulse analysis for control and monitoring applications
- **Timer Comparison:** Compare timer values for advanced event handling
- **Interrupt Support:** Generate CPU interrupts for precise system control and synchronization

Flexible and Technology-Independent Design

As with all DCD-SEMI IP Cores, the D6840 is **technology-independent**, enabling seamless implementation across **FPGA**, **ASIC**, and **SoC designs**. Its **modular architecture** allows easy integration into both legacy and modern embedded systems requiring reliable **timing, waveform generation, and measurement capabilities**.

Why Choose DCD-SEMI D6840 IP Core

- Compatible with **6840 industry standard**
- **Three 16-bit timers** with independent control and shared status
- Supports **square wave generation** with duty cycle control
- Enables **frequency/pulse width measurement and comparison**
- **Interrupt-driven operation** for CPU-controlled systems
- **Technology-independent** design for FPGA, ASIC, and SoC integration
- Ideal for **high-precision embedded applications**

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For integration support, technical specifications, or custom configurations, contact **info@dcd-semi.com**

KEY FEATURES

- Compatible with 6840 industry standard
- Three separate timers
- Two operation modes
  - Wave synthesis
  - Wave measurement
- Two generation modes
  - Continuous
  - Single shot
- Gating system for each clock input
- Separate timer outputs
- Prescaler mode for timer3 input clock
- External clock or E clock used for timer decrement
- Interrupt generation
- Split bus for input and output data
- Fully synthesizable
- Static synchronous design and no internal tri-states

DESIGN FEATURES

The functionality of the D6840 core was based on the MC6840. The following characteristics differentiate the D6840 from TI devices:

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- The IP core has an additional clock input, which is a main clock domain. The main clock is at least four times faster than the E clock. Typically, the main clock domain is the same as the clock for D68xx CPU which manages the D6840 module.
- Input E is treated as an input signal and synchronized to main clock domain. All counter events are related to the E signal, but are synchronized with the main clock domain. Typically, the E signal is connected from a D68xx CPU which manages the D6840 module.
- All latches implemented in original 6840 devices are replaced by equivalent flip-flop registers with the same functionality.

UNITS SUMMARY

CPU Interface – Performs access to internal registers from CPU. This module contains all control and status registers. There is also MSB and LSB buffer, used for access to 16-bit counter and Latch.
Timer1, 2, 3 – Main module, which contains 16-bit counter with all logic used for decrement, gating input clock and generating output signal and interrupt.
C3 Prescaler – clock divider for C3 input. Used for divide clock by 8 in pre-scaled mode of timer3.

APPLICATIONS

- External module for D68xx processors
- Gated wave generation
- Pulse width modulation
- Frequency measurement and comparison
- Pulse width measurement and comparison

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA** devices after Place & Route:

Device	Speed grade	LE/ALM	F_{max}
CYCLONE	-6	501	173 MHz
CYCLONE 2	-6	498	213 MHz
CYCLONE 3	-6	502	224 MHz
STRATIX	-5	501	168 MHz
STRATIX 2	-3	333	281 MHz
STRATIX 3	-3	330	384 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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