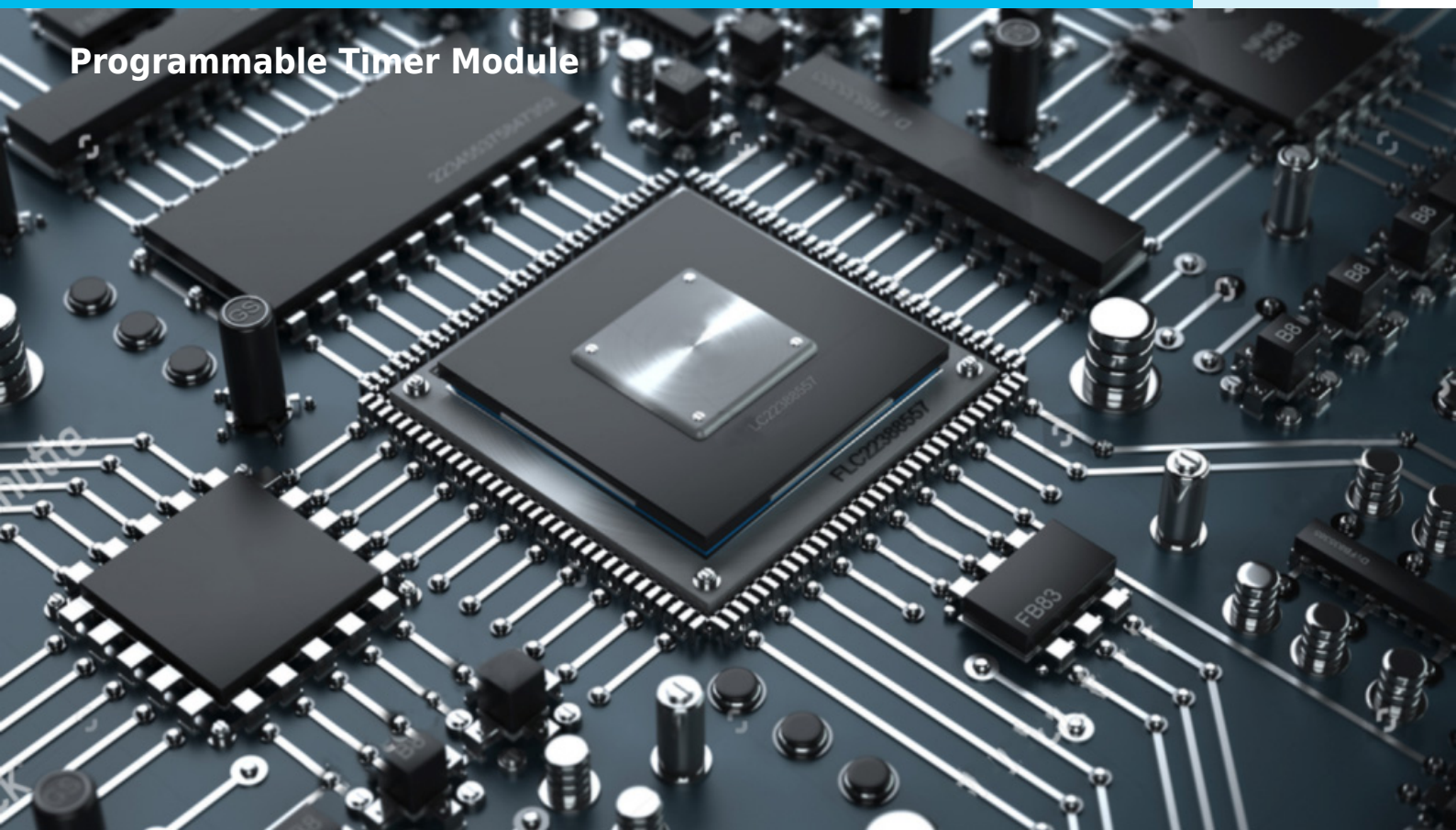
DIGITAL CORE DESIGN

D6840

Programmable Timer Module



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D6840 is a programmable timer module **compatible with the 6840 industry standard**. It was designed to be used in **peripheral devices for D68xx processors**. Moreover, our proprietary IP Core works perfectly as a **separate module in applications** where the 6840 timer features are useful. The D6840 has **three separate 16-bit timers** with individual control and common status registers. The timers may be used for square wave generation with duty cycle regulation. The signal may then be generated as a **continuous wave** or **single-shot mode**.
But this is not all – our unique module can be used **for frequency or pulse width measurement and comparison**. The D6840 has an interrupt which is used by the CPU in a controlling module. Like all of our solutions, the D6840 is a technology-independent design that can be implemented in a variety of process technologies.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.

- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

KEY FEATURES

- Compatible with 6840 industry standard
- Three separate timers
- Two operation modes
  - Wave synthesis
  - Wave measurement
- Two generation modes
  - Continuous
  - Single shot
- Gating system for each clock input
- Separate timer outputs
- Prescaler mode for timer3 input clock
- External clock or E clock used for timer decrement
- Interrupt generation
- Split bus for input and output data
- Fully synthesizable
- Static synchronous design and no internal tri-states

DESIGN FEATURES

The functionality of the D6840 core was based on the MC6840. The following characteristics differentiate the D6840 from TI devices:

- The IP core has an additional clock input, which is a main clock domain. The main clock is at least four times faster than the E clock. Typically, the main clock domain is the same as the clock for D68xx CPU which manages the D6840 module.
- Input E is treated as an input signal and synchronized to main clock domain. All counter events are related to the E signal, but are synchronized with the main clock domain. Typically, the E signal is connected from a D68xx CPU which manages the D6840 module.
- All latches implemented in original 6840 devices are replaced by equivalent flip-flop registers with the same functionality.

UNITS SUMMARY

CPU Interface – Performs access to internal registers from CPU. This module contains all control and status registers. There is also MSB and LSB buffer, used for access to 16-bit counter and Latch.
Timer1, 2, 3 – Main module, which contains 16-bit counter with all logic used for decrement, gating input clock and generating output signal and interrupt.
C3 Prescaler – clock divider for C3 input. Used for divide clock by 8 in pre-scaled mode of timer3.

APPLICATIONS

- External module for D68xx processors
- Gated wave generation
- Pulse width modulation
- Frequency measurement and comparison
- Pulse width measurement and comparison

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PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	Speed grade	LE/ALM	F_{max}
CYCLONE	-6	501	173 MHz
CYCLONE 2	-6	498	213 MHz
CYCLONE 3	-6	502	224 MHz
STRATIX	-5	501	168 MHz
STRATIX 2	-3	333	281 MHz
STRATIX 3	-3	330	384 MHz

DELIVEVERABLES

- **Source code:**
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- **Netlist**
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- **Technical support**
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

Digital Core Design Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/