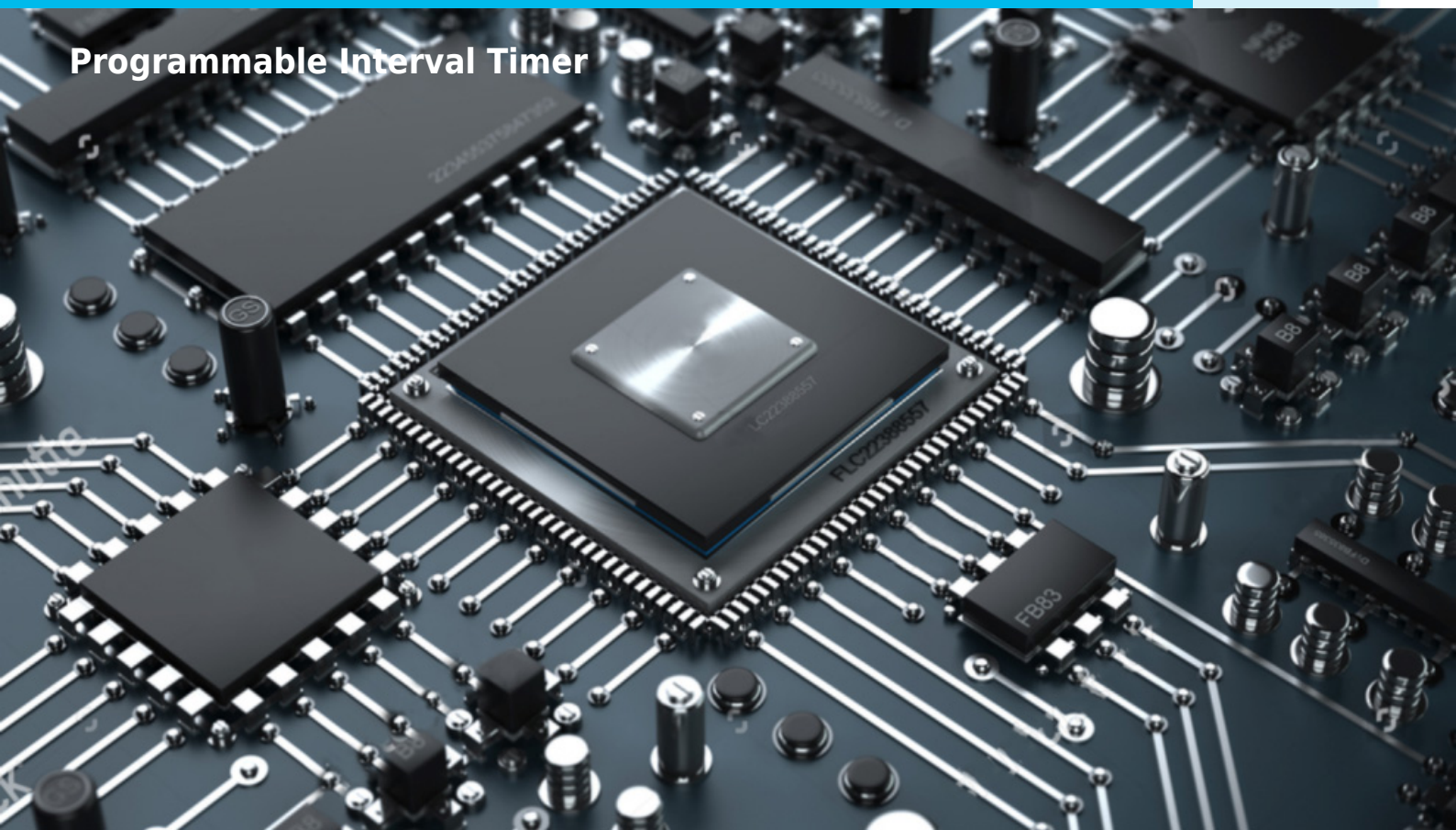
DIGITAL CORE DESIGN

D8254

Programmable Interval Timer



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D8254 IP Core — Programmable Interval Timer/Counter for Embedded Systems

High-Precision Timer and Counter IP Core

The **D8254 IP Core** from DCD-SEMI is a **programmable interval timer and counter**, fully **binary compatible with the 82C54 industry standard**. Designed for **high-precision timing applications**, it provides a reliable solution for generating **accurate time delays under software control**, a common challenge in microcomputer and embedded systems.

Versatile Applications

The D8254 can be configured for a wide variety of applications, including:

- **Real-Time Clock (RTC)**
- **Event Counter**
- **Digital One-Shot**
- **Programmable Rate Generator**
- **Square Wave Generator**
- **Binary Rate Multiplier**
- **Complex Waveform Generator**
- **Motor Controller Applications**
- **Interrupt on Terminal Count**

This flexibility makes the D8254 ideal for **SoC designs, FPGA implementations, and microcontroller-based systems**.

Advanced Features and Technology Independence

- **Automated Test Bench:** Includes a complete set of tests for **easy validation** during each stage of the SoC design flow
- **Technology-Independent Design:** Easily integrated into **FPGA, ASIC, or SoC platforms**
- **Binary Compatibility:** Ensures seamless replacement of the legacy **82C54 timer**

The D8254 combines **precision, reliability, and versatility**, empowering engineers to implement **complex timing and control functions** efficiently.

Why Choose DCD-SEMI D8254 IP Core

- Programmable **interval timer/counter** compatible with **82C54 standard**
- Supports a wide range of **timing and waveform generation applications**
- **Automated test bench** for fast verification and integration
- **Technology-independent design** for FPGA, ASIC, and SoC use
- Ideal for **real-time control, motor systems, and embedded microcomputer applications**

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For technical specifications, integration support, or customization options, contact **info@dcd-semi.com**

KEY FEATURES

- Three independent 16-bit counters
- Six programmable Counter modes
  - Interrupt on terminal count
  - Hardware retriggerable One-Shot
  - Rate Generator
  - Square wave mode
  - Software triggered strobe
  - Hardware triggered strobe
- Binary or BCD counting
- Status Read Back Command

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- Simple interface allows easy connection to microcontrollers
- Fully synthesizable
- Static design and no internal tri-states

APPLICATIONS

- Embedded microprocessor boards

UNITS SUMMARY

Read Write Logic – Accepts inputs from the system bus and generates control signals, for the other functional blocks of the D8254. ADDR(1:0) select one of the three counters or the Control Word Register, to be read from/written into. A “low” on the RD input tells the D8254, that the CPU is reading one of the counters. A “low” on the WR input tells the D8254 that the CPU is writing either a Control Word or an initial count. Both RD and WR are qualified by CS; RD and WR are ignored, unless the 82C54 has been selected by holding CS low. The WR and CLK signals should be synchronous. This is accomplished by using a CLK input signal to the D8254 counters, which is a derivative of the system clock source. Another technique is, to externally synchronize the WR and CLK input signals. This is done by gating WR with CLK.
Data Bus Buffer – This 8-bit buffer is used to interface the D8254 to the system bus.
Control Word – Selected by the Read/Write Logic when ADDR(1:0) = 11. If the CPU does a write operation to the D8254, the data is stored in the Control Word Register and is interpreted, as a Control Word used to define the operation of the Counters.
Status Register, Status Latch – Status register, which contains actual mode declaration and value of output signal. Latched in Status Latch, after receiving Read-Back Command with STATUS Bit = 0.
Control Unit – Controls read/write operation and decrementing of CE.
CR M, CR L – Input data registers. When a new count is written to counter, the count is written in the CR and later transferred to CE.
OL L, OL M – Output data registers. Latched when the suitable Counter Latch Command is sent to the D8254

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA** devices after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
Max 10	-8	618	155 MHz
Max V	-4	605	85 MHz
Arria V	-3	302	320 MHz
Cyclone V	-8	299 ALM	130 MHz
Stratix V	-3	291	350 MHz
Cyclone IV	-6	640	175 MHz
Stratix IV	-2	436	285 MHz
Cyclone III	-6	640	180 MHz
Stratix III	-2	435	295 MHz
Cyclone II	-6	620	166 MHz
Stratix II	-3	436	200 MHz
Cyclone	-6	610	134 MHz
Stratix	-6	610	134 MHz

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

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