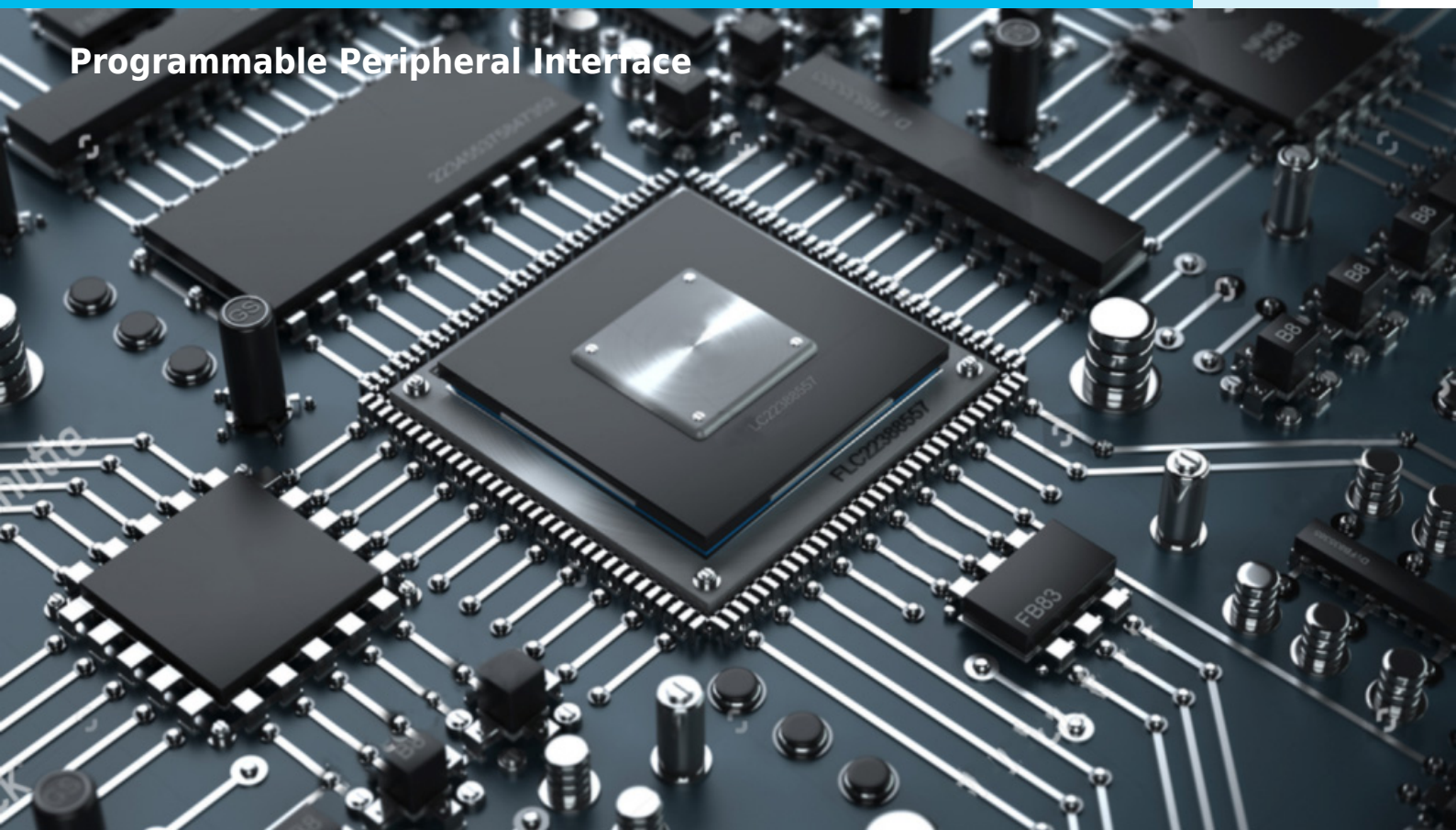
DIGITAL CORE DESIGN

D8255

Programmable Peripheral Interface



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D8255 is a **programmable I/O device** designed for use with all Intel CPUs. What's significant, it also supports most other microprocessors. Our innovative IP core provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation:

- **MODE 0** – **Basic Input/Output**. This functional configuration provides simple input and output operations for each of the three ports. No „handshaking" is required, data is simply written to or read from a specified port. Mode 0 Basic Functional Definitions:
  - Two 8-bit ports and two 4-bit ports,
  - Any port can be input or output,
  - 16 different Input/Output configurations are possible in this Mode.
- **MODE 1** – **Strobed Input/Output**. This functional configuration provides means for transferring I/O data to or from a specified port in conjunction with strobes or „handshaking" signals. In mode 1, Port A and Port B use the lines on Port C, to generate or accept these „handshaking" signals. Mode 1 Basic functional Definitions:
  - Two Groups (Group A and Group B).
  - Each group contains one 8-bit data port and one 4-bit control/data port.
  - The 8-bit data port can be either input or output Both inputs and outputs are latched.
  - The 4-bit port is used for control and status of the 8-bit data port.
- **MODE 2** – **Strobed Bidirectional Bus I/O**. This functional configuration provides means for communicating with a peripheral device or structure on a single 8-bit bus, both for transmitting and receiving data (bidirectional bus I/O). „Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available. MODE 2 Basic Functional Definitions:
  - Used in Group A only.
  - One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
  - The 5-bit control port (Port C) is used for control and status of the 8-bit, bi-directional bus port (Port A).

The functional configuration of the D8255 is programmed by the system software so that normally no external logic is needed to interface peripheral devices or structures.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

KEY FEATURES

- Compatible with industry standard 8255
- 24 I/O lines individually programmed in 2 groups of 12:
  - Group A – Port A and upper half of Port C
  - Group B – Port B and lower half of Port C
- 3 major modes of operation
  - Mode 0 – Basic input/output
  - Mode 1 – Strobed Input/output
  - Mode 2 – Bi-directional Bus
- Control Word Read-Back Capability
- Direct Bit Set/Reset Capability
- Interrupt control functions
- No internal three states busses
- Fully synthesizable, technology independent source code.

DESIGN FEATURES

- One global system clock
- Synchronous reset
- All asynchronous input signals are synchronized before internal use
- All latches implemented in original 8255 devices are replaced by equivalent flip-flop registers, with the same functionality

UNITS SUMMARY

Data Bus Buffer – The Data Bus Buffer is used to interface the D8255, to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions, by the CPU. Control words and status information are also transferred through the data bus buffer.
Read/Write and Control Logic – The control logic block manages all of the internal and external transfers of both, Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues

commands to both, A and B Control Groups.
Ports A, B, and C – The D8255 contains three 8-bit ports. All can be configured in a wide variety of functional characteristics by the system software, but each has its own special features or “personality”, for further enhancement of the power and flexibility of the D8255.
Port A – One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both „pull-up” and “pulldown” bus hold devices present on Port A.
Port B – One 8-bit data input/output latch/buffer. Only „pull-up” bus hold devices are present on Port B.
Port C – One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under mode control. Each 4-bit port contains a 4-bit latch and can be used for the control signal outputs and status signal inputs, in conjunction with ports A and B. Only „pull-up” bus hold devices are present on Port C.
Group A and Group B Controls – The functional configuration of each port is programmed by the systems software. In essence, the CPU “outputs” a control word to the D8255. The control word contains information, such as “mode”’, “bit set”, “bit reset”, etc., that initializes the functional configuration of the D8255. Each of the Control blocks (Group A and Group B), accepts “commands” from the Read/Write Control Logic, receives “control words” from the internal data bus and issues the proper commands to its associated ports.
– Group A – Port A and upper half of Port C
– Group B – Port B and lower half of Port C
The control word register can be both written and read. The figure on the right shows the control word format, for both Read and Write operations. When the control word is read, bit D7 will always be logic “1”, as this implies control word mode information.

APPLICATIONS

- Embedded microprocessor boards
- Interface to the printer
- I/O component to interface peripheral
- equipment to the microcomputer system bus

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	LE/ALM	F_{max}
CYCLONE IV GX	169	424 MHz
CYCLONE V	74	332 MHz
CYCLONE III	169	474 MHz
CYCLONE II	172	369 MHz
STRATIX V	74	800 MHz
STRATIX IV	119	710 MHz
STRATIX III	119	780 MHz
MAX V	164	144 MHz
MAX 10	167	335 MHz
CYCLONE 10LP	165	410 MHz
ARIA V	81	900 MHz

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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