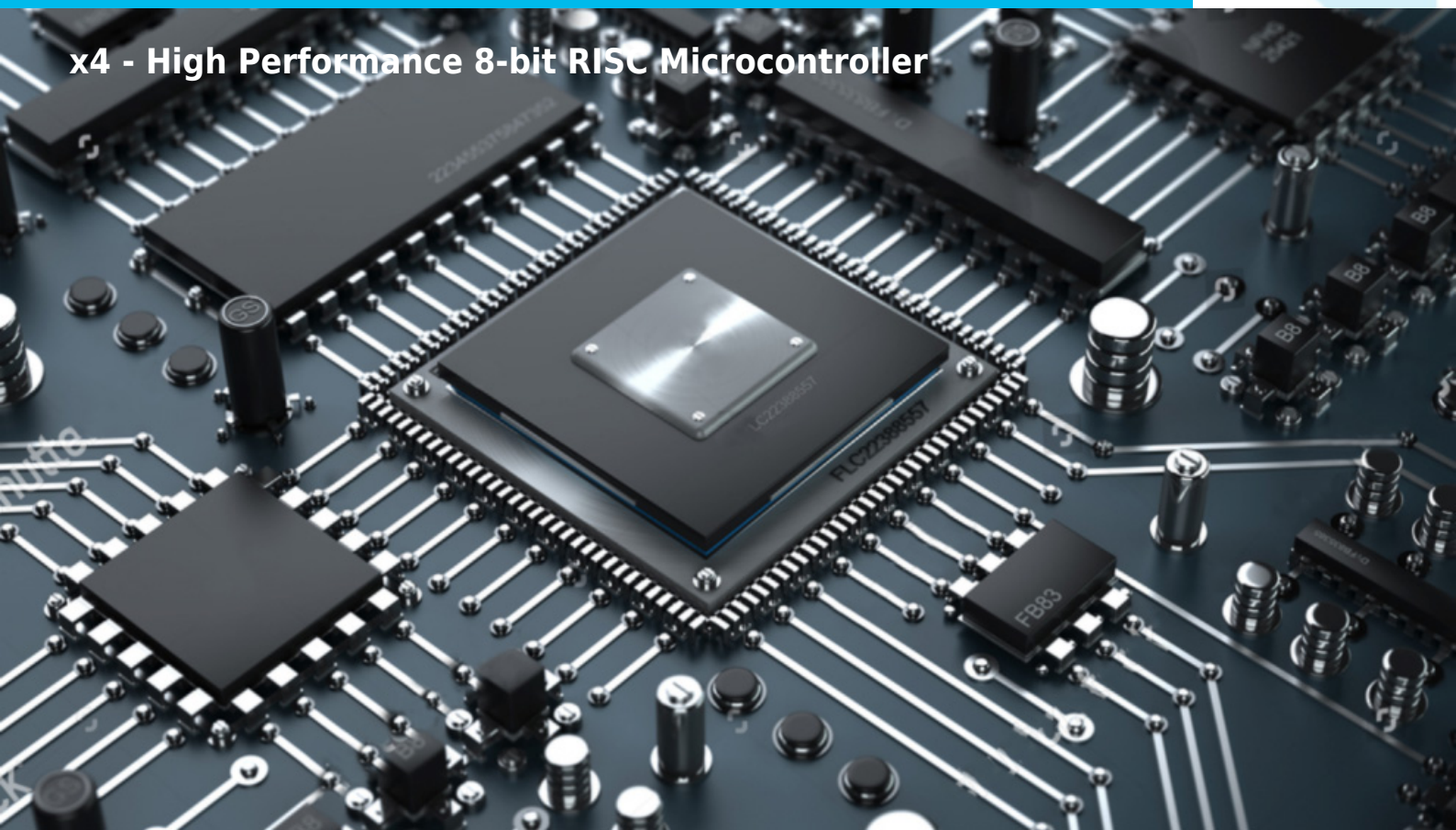
DIGITAL CORE DESIGN

DRPIC1655X

x4 - High Performance 8-bit RISC Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DRPIC1655X - LOW-POWER, HIGH-PERFORMANCE PIC16-COMPATIBLE 8-BIT CPU IP CORE

The **DRPIC1655X** is a **low-cost, high-performance, fully static 8-bit soft microcontroller IP core**, engineered for **SoC designs requiring PIC16 software compatibility**, **low power consumption**, and **efficient silicon utilization**.

Designed to operate with **fast, dual-ported memory**, the DRPIC1655X delivers an optimal **price-performance-power balance**, making it one of the most cost-effective **PIC-compatible CPU IP cores** available on the market. The core is **software-compatible with industry-standard PIC16XXX microcontrollers**, allowing reuse of existing firmware, development tools, and design expertise.

SOFTWARE COMPATIBILITY WITH PIC16XXX MICROCONTROLLERS

DRPIC1655X is **software-compatible with the PIC16 family**, enabling:

- Reuse of existing **PIC16 firmware and libraries**
- Familiar programming model and instruction set

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- Fast migration from discrete PIC MCUs to **ASIC or FPGA-based SoCs**

This compatibility significantly reduces **development risk, time-to-market, and software requalification effort**.

ENHANCED HARVARD ARCHITECTURE FOR HIGH-SPEED EXECUTION

The core implements an **enhanced Harvard architecture**, featuring:

- **Separate instruction and data memories**
- **Independent address and data buses**
- **14-bit program memory**
- **8-bit dual-ported data memory**

This architecture allows **simultaneous instruction fetch and data access**, enabling instruction execution and memory operations to occur in parallel.

Thanks to a **multi-stage pipeline**, the next instruction is fetched from program memory while the current instruction is executed using data from data memory — resulting in a **performance improvement of up to 4× compared to standard PIC16 architectures**.

EFFICIENT INSTRUCTION PIPELINE

- Most instructions execute in **a single system clock cycle**
- Instructions that directly modify the program counter (*GOTO, CALL, RETURN*) require one additional cycle due to pipeline refill
- Deterministic execution behavior suitable for real-time control systems

This predictable timing makes DRPIC1655X ideal for **control-oriented and timing-sensitive applications**.

ULTRA-LOW-POWER DESIGN WITH POWER-SAVE MODE

DRPIC1655X has been designed with **low power consumption as a primary goal**:

- Fully static implementation
- Built-in **power-save mode**
- Excellent performance-per-watt characteristics
- Ideal for **battery-powered and duty-cycled systems**

These features make the core especially suitable for **energy-constrained embedded applications**.

SOC-READY VERIFICATION AND NON-INTRUSIVE DEBUGGING

The DRPIC1655X is delivered with a **fully automated testbench and a complete regression test suite**, enabling **easy validation and fast integration** at every stage of the SoC design flow.

Each DRPIC1655X core includes built-in support for **DoCD™ (Digital Core Design on-Chip Debugger)** — a proprietary **real-time hardware debug system** that provides **full SoC visibility without disrupting application execution**.

DoCD™ Debug Capabilities

- Run, halt, single-step, step-over, and instruction skipping
- Read/write access to **all CPU registers and SFRs**, including user-defined peripherals
- Full access to **program and data memories**
- **True non-intrusive debugging** of running applications

KEY BENEFITS FOR DESIGN ENGINEERS

- PIC16XXX **software-compatible CPU IP**
- **Up to 4× faster** than standard PIC16 architectures
- Enhanced Harvard architecture with **dual-ported data memory**
- Fully static, **ultra-low-power design**

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- Built-in power-save mode
- Deterministic instruction timing
- Fully synthesizable **ASIC & FPGA-ready soft IP**
- **Non-intrusive SoC debugging** via DoCD™
- Complete verification environment included

TARGET APPLICATIONS

Automotive & Appliances

- Motor control systems
- Automotive actuators
- Appliance control electronics

Low-Power & Remote Devices

- Remote transmitters and receivers
- Wireless sensor nodes
- Battery-powered controllers

Consumer & Embedded

- Pointing devices and HID controllers
- Telecom and communication processors
- Cost-sensitive embedded systems

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com.

CPU FEATURES

- Software compatible with PIC16C55X industry standard
- Pipelined Harvard RISC architecture
  - **4 times faster, compared to original implementation**
- 35 instructions
- 14 bit wide instruction word
- **Up to 32 kB of internal Data Memory**
- **Up to 64K Words of Program Memory**
- Configurable hardware stack
- Power saving SLEEP mode
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- Technology independent HDL Source Code
- 800 MHz virtual clock frequency in a 0.35u technological process
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

PERIPHERALS

- **Four 8 bit I/O ports**
  - *Four 8-bit corresponding TRIS registers*
  - *Interrupt feature on PORTB(7:4) change*
- **Timer 0**
  - *8-bit timer/counter*
  - *Readable and Writable*
  - *8-bit software programmable prescaler*
  - *Internal or external clock select*
  - *Interrupt generation on timer overflow*
  - *Edge select for external clock*
- **Watchdog Timer**
  - *Configurable Time out period*
  - *7-bit software programmable prescaler*
  - *Dedicated independent Watchdog Clock input*
- **Extended Interrupt Controller**
  - *Three individually maskable Interrupt sources*
    - *External interrupt INT*
    - *Timer Overflow interrupt*
    - *Port B[7:4] change interrupt*
- **DoCD™ debug unit**
  - *Processor execution control*
    - *Run*
    - *Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
    - *Hardware Stack and Stack Pointer*
  - *Hardware execution breakpoints*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
  - *Three wire communication interface*

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OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented DRPIC1655X Microcontroller Core) are also available. The optional peripherals can be implemented upon customer's request.

- **Timer 1 and Timer 2**
- **Full duplex UART**
- **SPI – Master and Slave Serial Peripheral Interface**
  - *Supports speeds up ¼ of system clock*
    - *Mode fault error*
    - *Write collision error*
  - *Software selectable polarity and phase of serial clock SCK*
  - *System errors detection*
  - *Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)*
  - *Interrupt generation*
- **PWM – Pulse Width Modulation Timer**
  - 2 independent 8-bit PWM channels, concatenated on one 16-bit PWM channel
  - Software-selectable duty from 0% to 100% and pulse period
  - Software-selectable polarity of output waveform
- **I2C bus controller – Master**
  - 7-bit and 10-bit addressing modes
  - NORMAL, FAST, HIGH speeds
  - Multi-master systems supported
  - Clock arbitration and synchronization
  - User defined timings on I2C lines
  - Wide range of system clock frequencies
- **I2C bus controller – Slave**
  - NORMAL, FAST and HIGH Speed modes
  - Wide range of system clock frequencies
  - User defined data setup time on I2C lines

UNITS SUMMARY

ALU – Arithmetic Logic Unit – performs arithmetic and logic operations during execution of an instruction. Contains work register (W) and Status register.

Control Unit – Performs the core synchronization and data flow control. Manages execution of all instructions and carries out decode and control functions for all other blocks. Contains program counter (PC) and hardware stack.

Hardware Stack – It's a configurable hardware stack. The stack space is not a part of either program or data space and the stack pointer is neither readable, nor writable. The PC is pushed onto the stack, when CALL instruction is executed or an interrupt causes a branch. The stack is popped, while RETURN, RETFIE and RETLW instruction is executed. The stack operates, as a circular buffer – this means, that after the stack has been pushed eight times, the ninth push overwrites the value, that was stored from the first push.

RAM Controller – Performs interface functions between Data Memory and DRPIC16XXX internal logic. It assures correct Data Memory addressing and data transfers. The DRPIC16XXX supports two addressing modes: direct or indirect. In Direct Addressing, the 9-bit direct address is computed from RP(1:0) bits (STATUS) and from 7 least significant bits of instruction word. Indirect addressing is possible, by using the INDF register. Any instruction using INDF register, actually accesses data pointed to by the FSR (file select register). Reading INDF register indirectly, will produce 00h. Writing to the INDF register indirectly, results in a nonoperation. An effective 9-bit address is obtained, by concatenating the IRP bit (STATUS) and the 8-bit FSR register.

Interrupt Controller – Responsible for interrupt manage system for the external and internal interrupt sources. It contains interrupt related register, called INTCON. There are three interrupt sources:

– External interrupt INT
– TMR0 overflow interrupt
– PORTB change interrupt (pins B[7:4])

INTCON records individual interrupt requests in flag bits. A global interrupt enable (GIE) bit enables all unmasked interrupts. Each interrupt source has an individual enable bit, which can enable or disable corresponding interrupt. When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. The interrupt flag bits must be cleared in software before re-enabling interrupts.

Timer 0 – Main system's timer and prescaler, operates in two modes: 8-bit timer or 8-bit counter. In the "timer mode", timer/prescaler registers are incremented in every instruction cycle (1 or 2 CLK periods). When the prescaler is assigned into the TIMER, prescaler ratio can be divided by 2, 4, ..., 256. In the "counter mode", the timer register is incremented in every falling or rising edge of T0CKI pin, depending on T0SE bit in OPTION register.

Watchdog Timer– A free running timer. WDT has its own clock input, separate from system clock. It means, that the WDT will run, even if the system clock is stopped by execution of SLEEP instruction. During normal operation, a WDT timeout generates a Watchdog reset. If the device is in SLEEP mode, the WDT timeout causes the device to wake-up and continue with normal operation.

I/O Ports – This block contains general purpose I/O ports and data direction registers (TRIS). The DRPIC16XXX has four 8-bit full bi-directional ports PORT A, PORT B, PORT C, PORT D. Each port's bit can be individually accessed, by bit addressable instructions. Read and write accesses to the I/O port, are performed via their corresponding SFR's PORTA, PORTB, PORTC, PORTD. The reading instruction, always reads the status of Port pins. Writing instructions always write into the Port latches. Each port's pin has a corresponding bit in TRISA, B, C and D registers. When the bit of TRIS register is set, it means, that the corresponding bit of port is configured as an input (output drivers are set into the High Impedance).

DoCD™ Debug Unit – a **real-time hardware debugger,** which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurred at particular address, with certain data

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pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core, in real time debugging. It is built as scalable unit and some features can be turned off by the user to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to the power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off.

ARCHITECTURE IMPROVEMENT

Most instructions of the DRPIC1655X are executed within 1 CLK period, except program branches which require 2 CLK periods. The following table shows sample instructions execution times:

Mnemonic operands	DRPIC1655X (CLK cycles)	PIC16C554 (CLK cycles)	Impr.
ADDWF	1	4	4
ANDWF	1	4	4
RLF	1	4	4
BCF	1	4	4
DECFSZ	1(2)[1]	4(8)[1]	4
INCFSZ	1(2)[1]	4(8)[1]	4
BTFSC	1(2)[1]	4(8)[1]	4
BTFSS	1(2)[1]	4(8)[1]	4
CALL	2	8	4
GOTO	2	8	4
RETFIE	2	8	4
RETLW	2	8	4
RETURN	2	8	4

[1] number of clock in case when result of operation is 0.

PERFORMANCE

The following table gives a survey about the Core area and performance in **AMD FPGA** devices after Place & Route:

Device	Speed grade	Slices	F_{max}
VIRTEX-IV	-12	483	109 MHz
VIRTEX-IIP	-7	483	102 MHz
VIRTEX-II	-6	484	86 MHz
VIRTEX-E	-8	474	51 MHz
VIRTEX	-6	474	41 MHz
SPARTAN-IIIE	-4	489	45 MHz
SPARTAN-III	-5	483	59 MHz
SPARTAN-IIE	-7	473	47 MHz
SPARTAN-II	-6	474	43 MHz

The area utilized by each unit of the DRPIC1655X core in vendor specific technologies is summarized in the following table.

Component	AREA	
	[Slices]	[FFs]
CPU*	363	285
Timer 0	38	29
Watchdog Timer	32	38
I/O Ports	50	64
Total area	**483**	**416**

* CPU – consisted of ALU, Control Unit, Bus Controller, Hardware Stack, Extended interrupt controller, External INT pin Interrupt Controller, Extended Interrupt controller, 512 B of RAM 8kW of program memory

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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