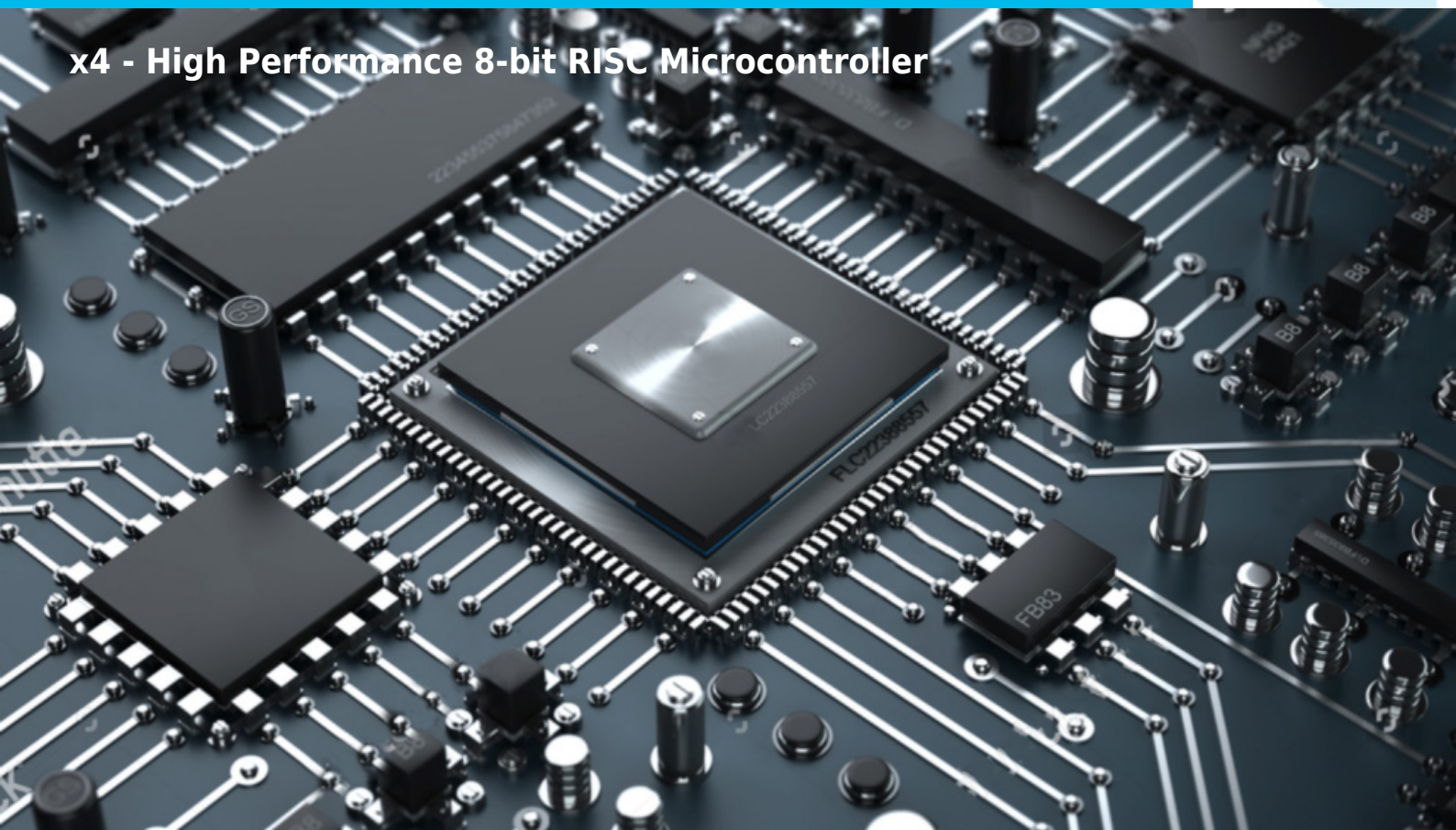
DIGITAL CORE DESIGN

DRPIC166X

x4 - High Performance 8-bit RISC Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DRPIC166X is a **low-cost**, **high-performance**, 8-bit, fully static soft IP Core, intended to operate with fast (typically on-chip) dual-ported memory. The core was designed with a special concern about low power consumption, assuring **the best power use, price, and performance combination** available on the market. The DRPIC166X softcore is software-compatible with industry-standard PIC 16XXX Microcontrollers. It implements an enhanced **Harvard architecture** (separate instruction and data memories) with independent address and data buses. The 14-bit program memory and 8-bit dual port data memory allow instruction fetch and data operations to occur simultaneously. The advantage of this architecture is that the instruction fetch and memory transfers can be overlapped by a multi-stage pipeline so that the next instruction can be fetched from program memory, while the current instruction is executed with data from the data memory. The DRPIC166X architecture is **4 times faster compared to the standard architecture.** Most instructions are executed within 1 system clock period, except instructions that directly operate on the PC (GOTO, CALL, RETURN) program counter. This situation requires the pipeline to be cleared and subsequently refilled. This operation takes an additional one clock cycle.

The DRPIC166X Microcontroller fits perfectly in applications ranging from high-speed automotive and appliance motor control, to low-power, remote transmitters/receivers, pointing devices, and telecom processors. Built-in power save mode makes this IP core perfect for applications where the power consumption aspect is critical. The DRPIC166X is delivered with a **fully automated test bench** and a **complete set of tests**, allowing easy package validation at each stage of the SoC design flow. Each of DCD's PIC Cores has built-in support for a Hardware Debug System called **DoCD™** – a **real-time hardware debugger**, which provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides non-intrusive debugging of a running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, and SFRs, including user-defined peripherals and data and program memories.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.
- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

CPU FEATURES

- Software compatible with PIC16C6X industry standard
- Pipelined Harvard RISC architecture
  - **4 times faster**, compared to original implementation
- 35 instructions
- 14 bit wide instruction word
- **Up to 32 kB of internal Data Memory**
- **Up to 64 K Words of Program Memory**
- Configurable hardware stack
- Power saving SLEEP mode
- Fully synthesizable
- Static synchronous design
- Positive edge clocking and no internal tri-states
- Scan test ready
- Technology independent HDL Source Code
- 800 MHz virtual clock frequency in a 0.35u technological process
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

PERIPHERALS

- **Four 8 bit I/O ports**
  - *Four 8-bit corresponding TRIS registers*
  - *Interrupt feature on PORTB(7:4) change*
- **Timer 0**
  - *8-bit timer/counter*
  - *Readable and Writable*
  - *8-bit software programmable prescaler*
  - *Internal or external clock select*
  - *Interrupt generation on timer overflow*
  - *Edge select for external clock*
- **Timer 1**
  - *16-bit timer/counter*
  - *3-bit prescaler*
  - *Internal or external clock select*
  - *Interrupt generation on timer overflow*
- **Timer 2**
  - 8-bit timer with prescaler
- **CCP – Compare-Capture-PWM**
  - *16 Bit Compare/Capture operations*
  - *10-bit resolution PWM output*
- **USART**
  - *Asynchronous – full duplex*
  - *Synchronous – half duplex Master/Slave*
- **Watchdog Timer**

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- *Configurable Time out period*
- *7-bit software programmable prescaler*
- *Dedicated independent Watchdog Clock input*

- **Interrupt Controller**
  - *Seven individually maskable Interrupt sources*
    - *Two external interrupts – INT Port B[7:4] change*
    - *Five internal interrupts–TIMERS 0, 1, 2, USART*
- **DoCD™ debug unit**
  - *Processor execution control*
    - *Run*
    - *Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
    - *Hardware Stack and Stack Pointer*
  - *Hardware execution breakpoints*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
  - *Three wire communication interface*

OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented DRPIC166X Microcontroller Core) are also available. The optional peripherals can be implemented upon customer's request.

- **SPI – Master and Slave Serial Peripheral Interface**
  - *Supports speeds up ¼ of system clock*
    - *Mode fault error*
    - *Write collision error*
  - *Software selectable polarity and phase of serial clock SCK*
  - *System errors detection*
  - *Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)*
  - *Interrupt generation*
- **I2C bus controller – Master**
  - *7-bit and 10-bit addressing modes*
  - *NORMAL, FAST, HIGH speeds*
  - *Multi-master systems supported*
  - *Clock arbitration and synchronization*
  - *User defined timings on I2C lines*
  - *Wide range of system clock frequencies*
- **I2C bus controller – Slave**
  - *NORMAL, FAST and HIGH speed modes*
  - *Wide range of system clock frequencies*
  - *User defined data setup time on I2C lines*

UNITS SUMMARY

ALU – Arithmetic Logic Unit – performs arithmetic and logic operations during execution of an instruction. This module contains work register (W) and Status register.
Control Unit – It performs the core synchronization and data flow control. This module manages execution of all instructions. It carries out the decode and control functions for all other blocks. It contains program counter (PC) and hardware stack.
Hardware Stack – It's a configurable hardware stack. The stack space is not a part of either program or data space and the stack pointer is neither readable, nor writable. The PC is pushed onto the stack, when CALL instruction is executed or an interrupt causes a branch. The stack is popped, while RETURN, RETFIE and RETLW instruction is executed. The stack operates, as a circular buffer – this means, that after the stack has been pushed eight times, the ninth push overwrites the value, that was stored from the first push.
RAM Controller – It performs interface functions between Data Memory and DRPIC16XXX internal logic. It assures correct Data Memory addressing and data transfers. The DRPIC16XXX supports two addressing modes: direct or indirect. In Direct Addressing, the 9-bit direct address is computed from RP(1:0) bits (STATUS) and from 7 least significant bits of instruction word. Indirect addressing is possible, by using the INDF register. Any instruction using INDF register, actually accesses data pointed to by the FSR (file select register). Reading INDF register indirectly, will produce 00h. Writing to the INDF register indirectly, results in a nonoperation. An effective 9-bit address is obtained, by concatenating the IRP bit (STATUS) and the 8-bit FSR register.
Timer 0 – Main system's timer and prescaler. It operates in two modes: 8-bit timer or 8-bit counter. In the "timer mode", timer/prescaler registers are incremented in every instruction cycle (1 or 2 CLK periods). When the prescaler is assigned into the TIMER, prescaler ratio can be divided by 2, 4, ..., 256. In the "counter mode", the timer register is incremented in every falling or rising edge of T0CKI pin, depending on T0SE bit in OPTION register.
Timer 1 – It is a 16-bit timer, consisting of two 8-bit registers (TMR1H and TMR1L). Timer 1 can operate either as a 16 bit timer (incremented in every CLK clock period) or as a Counter, incremented by rising edge on the T1CKI input pin. The Timer1 interrupt is generated by the timer overflow.
Timer 2 – It is a 8-bit Timer with a prescaler and postscaler. Timer2 is suitable as PWM time-base. The Timer2 module has an 8-bit period register (PR2). Timer2 is incremented, until it matches PR2 and then resets on the next increment cycle. The match output of the TMR2 register goes through a 4-bit postscaler, to generate a TMR2 interrupt.
Interrupt Controller – Interrupt Controller module is responsible for interrupt management system for the external and internal interrupt sources. It contains interrupt related registers, called INTCON, PIE1, PIR1. There are seven individually maskable interrupt sources:

– Two external interrupts – INT pin, PORTB change (pins B7:B4)
– Five internal interrupts – Timers 0, 1, 2, USART, CCP1

The interrupt control register INTCON and PIR1 records individual interrupt requests in flag bits. A global interrupt enable bit, GIE and Peripheral interrupts enable bit, PIE enables all unmasked interrupts. Each interrupt source has an individual enable bit, which can enable or disable corresponding interrupt. When an interrupt is responded to, the GIE is cleared, to disable any further interrupt, the return

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address is pushed into the stack and the PC is loaded with 0004h. The interrupt flag bits must be cleared in software, before re-enabling interrupts.

I/O Ports – The ports block contains general purpose I/O ports and data direction registers (TRIS). The DRPIC16XXX has four 8-bit full bi-directional ports PORT A, PORT B, PORT C, PORT D. Each port's bit can be individually accessed, by bit addressable instructions. Read and write accesses to the I/O port, are performed via their corresponding SFR's PORTA, PORTB, PORTC, PORTD. The reading instruction, always reads the status of Port pins. Writing instructions always write into the Port latches. Each port's pin has an corresponding bit in TRISA, B, C and D registers. When the bit of TRIS register is set, it means, that the corresponding bit of port is configured as an input (output drivers are set into the High Impedance).

CCP/PWM – The CCP module contains a 16-bit register, which can operate as a 16-bit capture register, 16-bit compare register or as a PWM master/slave duty cycle register.

Watchdog Timer– The watchdog timer is a free running timer. WDT has its own clock input, separate from system clock. It means, that the WDT will run, even if the system clock is stopped by execution of SLEEP instruction. During normal operation, a WDT timeout generates a Watchdog reset. If the device is in SLEEP mode, the WDT timeout causes the device to wake-up and continue with normal operation.

USART – The **Universal Synchronous Asynchronous Receiver Transmitter** module is also known as a Serial Communication Interface (SCI). The USART can be configured as a full duplex asynchronous system, that can communicate with peripheral devices or it can be configured as a half-duplex synchronous system (Master or Slave).

DoCD™ Debug Unit – it's a **real-time hardware debugger,** which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurred at particular address, with certain data pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core, in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When the debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

IMPROVEMENT

Most instructions of DRPIC166X are executed within 1 CLK period, except program branches which require 2 CLK periods. The following table shows sample instructions execution times:

Mnemonic operands	DRPIC166X (CLK cycles)	PIC16C6X (CLK cycles)	Impr.
ADDWF	1	4	4
ANDWF	1	4	4
RLF	1	4	4
BCF	1	4	4
DECFSZ	1(2)[1]	4(8)[1]	4
INCFSZ	1(2)[1]	4(8)[1]	4
BTFSC	1(2)[1]	4(8)[1]	4
BTFSS	1(2)[1]	4(8)[1]	4
CALL	2	8	4
GOTO	2	8	4
RETFIE	2	8	4
RETLW	2	8	4
RETURN	2	8	4

1- number of clock in case that result of operation is 0.

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route:

Device	Speed grade	LE/ALM	F_{max}
CYCLONE	-6	1 654	81 MHz
CYCLONE II	-6	1 654	72 MHz
STRATIX	-5	1 655	86 MHz
STRATIX II	-3	1 401	166 MHz
STRATIX GX	-5	1 655	84 MHz
APEX II	-7	1 695	74 MHz
APEX20KC	-7	1 695	64 MHz
APEX20KE	-1	1 695	54 MHz
APEX20K	-1	1 695	50 MHz
ACEX1K	-1	1 695	52 MHz
FLEX10KE	-1	1 695	54 MHz

The area utilized by each unit of the DRPIC166X core in vendor specific technologies is summarized in the following table.

Component	Area	
	[LE]	[FFs]
CPU*	904	296
Timer 0	60	29
Timer 1	81	30
Timer 2	90	34
USART	257	100
CCP1	111	32
Watchdog Timer	55	38
I/O Ports	96	64
Total area	1 654	625

*CPU – consisted of ALU, Control Unit, Bus Controller, Hardware Stack, External INT pin Interrupt Controller, Extended interrupt controller (512 Bytes RAM and 8kW of program memory)

DELIVEVERABLES

- Source code:

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- VERILOG or VHDL Source Code
- VERILOG or VHDL test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application

- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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