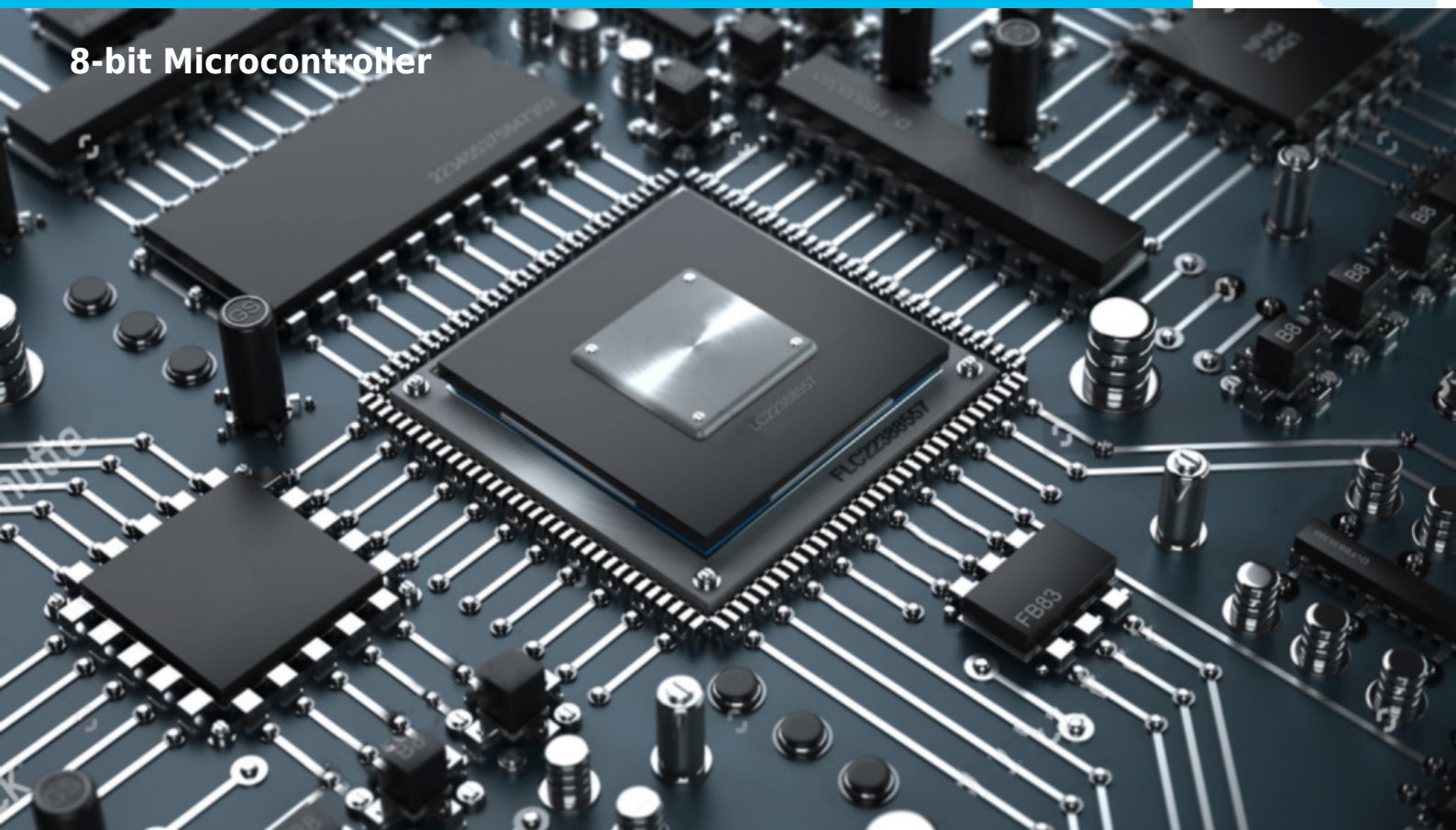
DIGITAL CORE DESIGN

D68HC11K

8-bit Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D68HC11K is synthesizable soft IP Core Microcontroller, fully compatible with the industry standard. It can be used as **a direct replacement for the following Motorola MC68HC11K microcontrollers:**

- **MC68HC11K0**
- **MC68HC11K1**
- **MC68HC11K4**
- **MC68HC711K4**
- **MC68HC11KS2**
- **MC68HC711KS2**

In a standard configuration of the core, major peripheral functions are integrated on-chip. An asynchronous serial communication interface (SCI) and a separate synchronous serial peripheral interface (SPI) are included. The main 16-bit, free-running timer system, contains input capture and output-compare lines and a real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods. The memory expansion unit (with six address extension lines) allows up to sixteen 32K byte banks of external memory to be addressed in either of two bank windows. The MEU extension of memory space can be up to 1MB. Self-monitoring on-chip circuitry is included, to protect the D68HC11K against system errors. The Computer Operating Properly (COP) watchdog system protects against software failures. An illegal opcode detection circuit provides a non-maskable interrupt if an illegal opcode is detected. Two software-controlled power-saving modes – WAIT and STOP are available, to preserve additional power. These modes make the D68HC11K IP Core especially attractive for **automotive and battery-driven applications.** The D68HC11K Microcontroller Core can be equipped with an ADC Controller, allowing the use of an external ADC Controller with standard ADC software. The ADC Controller makes external ADCs visible as internal ADCs in original 68HC11K Microcontrollers. The D68HC11K is fully customizable – it is delivered in the exact configuration to meet your requirements. There is no need to pay extra for unused features and wasted silicon. The D68HC11K comes with a **fully automated test bench** and a **complete set of tests**, allowing easy package validation at each stage of the SoC design flow. Each DCD's DF68XX and D68HC11X Core has built-in support for DCD's Hardware Debug System called **DoCD™**. It is a **real-time hardware debugger** that provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides **non-intrusive debugging** of a running application. It can halt, run, step into or skip an instruction, and read/write any contents of the microcontroller, including all registers and SFRs, including user-defined peripherals, data, and program memories.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.

- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

CPU FEATURES

- Cycle compatible with original implementation
- Software compatible with 68HC11K industry standard
- I/O Wrapper, making it pin-compatible core
- SFR registers remapped to any 4KB memory page
- Two power saving modes: STOP, WAI
- Fully synthesizable
- Static synchronous design
- No internal tri-states
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

- One global system clock
- Synchronous reset
- All asynchronous input signals are synchronized before internal use

PERIPHERALS

The peripherals listed below are implemented in a standard configuration of the D68HC11K.

- **DoCD™ On-Chip Debugger**
  - Processor execution control
  - Read, write all processor contents
  - Hardware execution breakpoints
  - Three wire communication interface
- **I/O Ports**
- **Interrupt Controller**

- Dedicated vector and interrupt priority for each interrupt source
- **Main 16-bit timer/counter system**
  - 16 bit free running counter
  - Four stage programmable prescaler
  - Real Time Interrupt
- **16-bit Compare/Capture Unit**
  - Three independent input-capture
  - Five output-compare channels
  - Events capturing
  - Pulses and digital signals generation
  - Gated timers
  - Sophisticated comparator
- 8-bit Pulse accumulator
  - Two major modes of operation
  - Simple event counter
  - Gated time accumulation
  - Clocked by internal source or external pin
- **SPI – Master and Slave Serial Peripheral Interface**
  - Software selectable polarity and phase of serial clock SCK
  - System errors detection
  - Allows operation from a wide range of system clock frequencies (built-in 5-bit timer)
  - Interrupt generation
- **Full-duplex UART – SCI**
  - Standard non-return-to-zero format
  - 8 or 9 bit data transfer
  - Integrated baud rate generator
  - Noise, Overrun and Framing error detection
  - IDLE and BREAK characters generation
  - Wake-up block to recognize UART wake-up from IDLE condition
  - Three SCI related interrupts
  - PWM – Modulation Timer/Counter
  - Memory extension unit and Chip select

OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented D68HC11K Microcontroller Core) are also available. The optional peripherals can be implemented upon customer's request.

- **I2C Master & Slave bus controllers**
  - Master operation
  - Multi-master systems supported
  - Performs arbitration and clock synchronization
  - Interrupt generation
  - Supports speed up to 3,4Mb/s (standard, fast & HS modes)
  - Allows operation from a wide range of clock frequencies (build-in 8-bit timer)
  - User-defined timing
- **Floating-Point Arithmetic Coprocessor (DFPAU) IEEE-754 standard single precision**
  - FADD, FSUB – addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM – compare
  - FCHS – change sign
  - FABS – absolute value
- **Floating-Point Math Coprocessor (DFPMU) – IEEE-754 standard single precision real, word and short integers**
  - FADD, FSUB- addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM- compare
  - FCHS – change sign
  - FABS – absolute value
  - FSIN, FCOS- sine, cosine
  - FPTAN, FPATAN- tangent, arcs tangent
- **Additional special internal interrupt dedicated for DFPAU or DFPMU**

UNITS SUMMARY

Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions, execution of STOP instruction and waking the processor up from the STOP mode.
Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks.
ALU – Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index registers X, Y and related logic like arithmetic unit, logic unit, multiplier and divider.
Bus Controller – Program Memory, Data Memory & SFR's (Special Function Register) interface controls access into the program and data memories and special registers. It contains Program Counter (PC), Stack Pointer (SP) register, and related logic.
Interrupt Controller – D68HC11 extended IC has implemented 17-level interrupt priority control. The interrupt requests may come from external pins (IRQ and XIRQ), as well as from particular peripherals. The D68HC11 peripheral systems generate maskable interrupts, which are recognized only, if the global interrupt mask bit (I) in the CCR is cleared. Maskable interrupts are prioritized according to default arrangement, established during reset. However, any source may be elevated to the highest maskable priority position, by using HPRIO register. When interrupt condition occurs, an interrupt status flag is set, to indicate the condition.
Timer, Compare Capture & COP Watchdog – This timer system is based on a free-running, 16-bit counter with a 4-stage programmable prescaler. A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. Three independent input-capture functions are used to automatically record the time, when a selected transition is detected at respective timer input pin. Five output-compare functions are included for generating output signals or for timing software delays. Since the input-capture and output-compare functions may not be familiar to all users, these concepts are explained in greater detail. A programmable periodic interrupt circuit called RTI, is tapped off of the main 16-bit timer counter. The software can select one of four rates for the RTI, which is most commonly used to pace the execution of software routines. The COP watchdog function is loosely related to the main

timer, in that the clock input to the COP system (clk*2^{17}) is tapped off the free-running counter chain. The timer subsystem involves more registers and control bits than any other subsystem on the MCU. Each of the three input-capture functions has its own 16-bit time capture latch (input-capture register), and each of the five output-compare functions has its own 16-bit compare register. All timer functions, including the timer overflow and RTI, have their own interrupt controls and separate interrupt vectors. Additional control bits, permit software to control the edge(s) that trigger each input-capture function and automatic actions that result from output-compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is mainly a software-oriented system. This structure is easily adaptable to a very wide range of applications, although it is not as efficient, as a dedicated hardware for some specific timing applications.

SCI – The SCI is a full-duplex UART type asynchronous system, using standard non return to zero (NRZ) format : 1 start bit, 8 or 9 data bits and a 1 stop bit. The D68HC11E resynchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore, differences in baud rate between the sending device and the SCI are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time and majority logic decides the sense for the bit. The receiver also has the ability to enter a temporary standby mode (called receiver wakeup), to ignore messages intended for a different receiver. Logic automatically wakes the receiver up, in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multi-drop SCI networks. The SCI transmitter can produce queued characters of idle (whole characters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag, this SCI also provides a transmit complete (TC) indication, that can be used in applications with a modem.

SPI Unit – it's a fully configurable master/slave Serial Peripheral Interface, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications, in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols, to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates, for the serial clock. SPI automatically drives slave select outputs SSO[7:0] and address SPI slave device to exchange serially shifted data. Error-detection logic is included, to support interprocessor communications. A write-collision detector indicates, when an attempt is made to write data to the serial shift register, while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers, if more than one SPI devices simultaneously attempt to become bus master.

Pulse Accumulator – This system is based on an 8-bit counter and can be configured, to operate as a simple event counter or for gated time accumulation. Unlike the main timer, the 8-bit pulse accumulator counter can be read or written at any time (the 16-bit counter in the main timer cannot be written). Control bits allow the user to configure and control the pulse accumulator subsystem. Two maskable interrupts are associated with the system, each having its own controls and interrupt vector. The PAI pin associated with the pulse accumulator can be configured to act as a clock (event counting mode) or as a gate signal, to enable a free-running E divided by 64 clock to the 8-bit counter (gated time accumulation mode). The alternate functions of the pulse accumulator input (PAI) pin, present some interesting application possibilities.

I/O Ports – All ports are 8-bit general-purpose bi-directional I/O system. The PORTA, PORTB, PORTC, PORTD, PORTE, PORTF and PORTG data registers have their corresponding data direction registers DDRX to control ports data flow. It assures that all D68HC11's ports have full I/O selectable registers. Writes to any ports pins cause data to be stored in the data registers. If any port pins are configured as output then data registers are driven out of those pins. Reads from port pins configured as input causes that input pin is read. If port pins is configured as output, during read data register is read. Writes to any ports pins not configured as outputs, do not cause data to be driven out of those pins, but the data is stored in the output registers. Thus, if the pins later become outputs, the last data written to port will be driven out the port pins.

ADCCTRL – External ADC Controller is used as an interface, between D68HC11 internal registers and external serial/parallel ADC converter. This module has several different options, so its details are described in separate document.

EEPROMCTRL – External Serial EEPROM controller. Manages data exchange between D68HC11 and external EEPROM. During initialization, copies contents of whole external EEPROM to internal EEPRAM (EEPROM Mirror implemented in standard parallel RAM). This module has several different options, so its details are described in separate document.

DoCD™ – Debug Unit – it's a real-time hardware debugger, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal, external, program memories, all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off. The separate CLKDOCD

clock line allows the debugger to operate while the CPU is in STOP mode and the major clock line CLK is stopped.
Memory expansion – This unit is able to extend the memory space beyond the physical 64kB.
TIMER 2 – Timer 2 is available in D68HC11KW1 only, it comprises a 4-stage prescaler and a 16-bit counter. It has three associated 16-bit output compare registers, along with a software-programmable input capture or output compare register. The functions of Timer 2 share I/O with the pins of port J.
TIMER 3 – Timer 3 is available in D68HC11KW1 only, it comprises a 4-stage prescaler and a 16-bit counter. It has three associated 16-bit output compare registers, along with a software-programmable input capture or output compare register. The functions of Timer 3 share I/O with the pins of Port K

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- ***Lattice,***
- ***Microsemi / Microchip, and others.***

- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

PERFORMANCE

The following table gives a survey about the Core area and performance in **XILINX®** devices after Place & Route:

Device	Speed grade	Slices	F_{max}
SPARTAN2E	-7	2 727	25 MHz
SPARTAN3	-5	2 648	37 MHz
SPARTAN3E	-5	2 648	35 MHz
VIRTEX	-6	2 649	24 MHz
VIRTEX2	-5	2 705	50 MHz
VIRTEX4	-11	2 635	56 MHz

D68HC11K4 Core performance in XILINX® devices

Device	Speed grade	Slices	F_{max}
SPARTAN2E	-7	3 136	28 MHz
SPARTAN3	-5	3 126	38 MHz
SPARTAN3E	-5	3 126	37 MHz
SPARTAN3A	-5	3 128	35 MHz
VIRTEX	-6	3 140	24 MHz
VIRTEX2	-5	3 146	38 MHz
VIRTEX4	-12	3 130	56 MHz
VIRTEX5	-3	1 816	71 MHz

D68HC11KW1 Core performance in XILINX® devices

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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