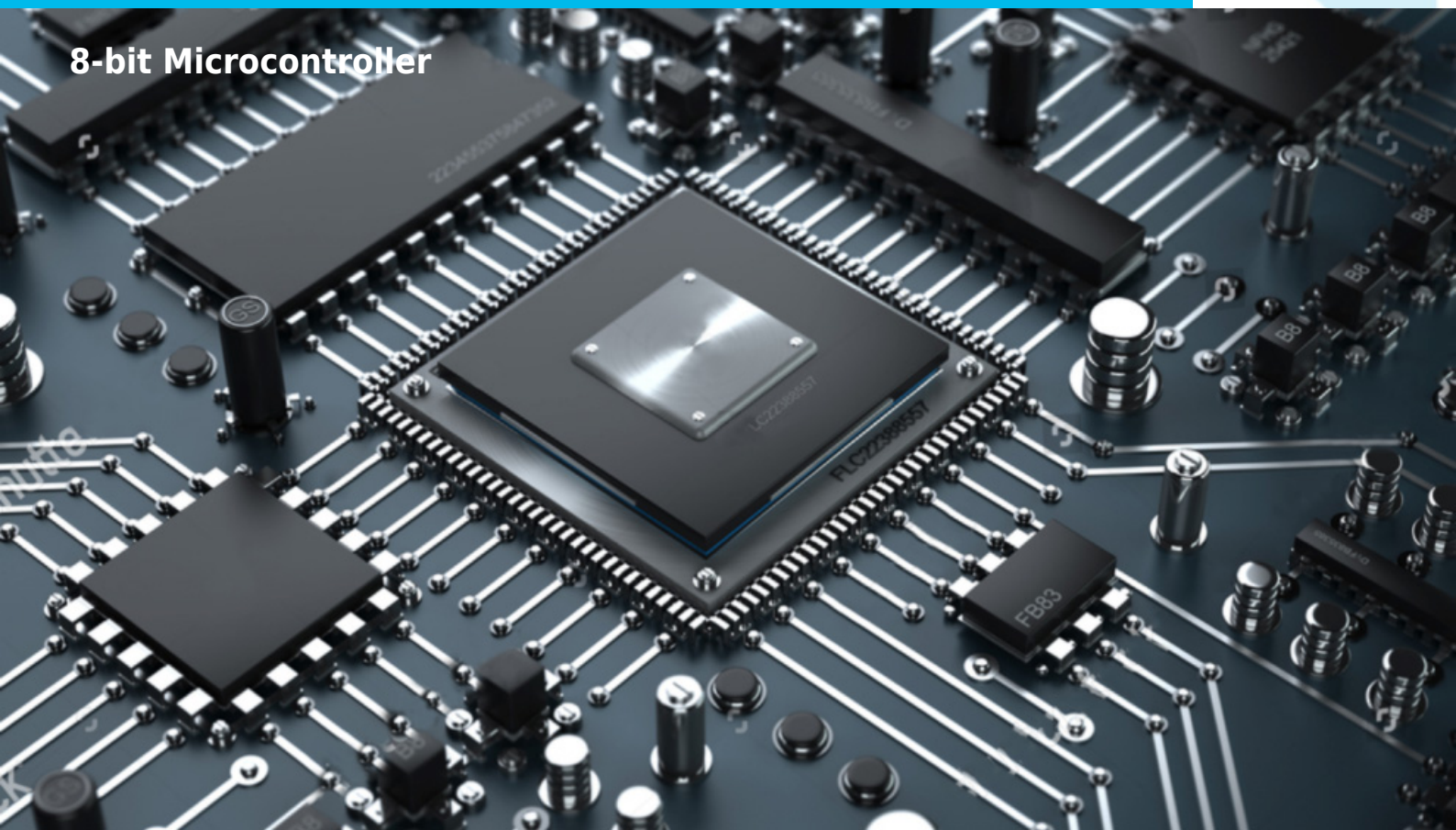
DIGITAL CORE DESIGN

D68HC11F

8-bit Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

D68HC11F 8-BIT MCU IP CORE – FULLY COMPATIBLE 68HC11F1 REPLACEMENT FOR MODERN SOCS

The **D68HC11F** is a fully synthesizable **8-bit Microcontroller IP Core**, offering **100% binary compatibility** with the industry-standard **Motorola 68HC11F1** microcontroller. Designed as a **drop-in replacement**, it enables seamless reuse of existing firmware while extending the classic 68HC11F1 architecture into modern, cost-effective **System-on-Chip (SoC)** implementations.

In its standard configuration, the D68HC11F integrates all key peripheral functions on-chip, making it ideal for **automotive, battery-powered, and industrial embedded systems** that demand deterministic behavior, long-term availability, and proven software compatibility.

Key Features and Capabilities

- **Full 68HC11F1 Compatibility**
  Executes unmodified legacy software with identical instruction set behavior and register mapping.

- **Integrated Serial Interfaces**
  Includes an asynchronous **SCI** and a synchronous **SPI**, ensuring flexible communication with external devices.

- **Advanced Timer Subsystem**
  A 16-bit free-running timer with **input capture**, **output compare**, and **real-time interrupt** support for precise control applications.

- **Pulse Accumulator**
  8-bit pulse accumulator capable of counting external events or measuring signal periods.

- **Reliability and Safety Mechanisms**
  On-chip self-monitoring circuitry, **COP watchdog**, and illegal opcode detection with **non-maskable interrupt (NMI)** enhance system robustness.

- **Low-Power Operation**
  Software-controlled **WAIT** and **STOP** modes reduce power consumption, making the core well suited for energy-sensitive designs.

- **Optional ADC Controller Support**
  Allows external ADCs to appear as internal ADCs, preserving compatibility with standard 68HC11F1 ADC software.

- **Fully Customizable Architecture**
  Delivered in an exact configuration matching project requirements—no unnecessary logic, no wasted silicon, no extra licensing cost.

- **SoC-Ready Verification**
  Supplied with a **fully automated testbench** and comprehensive verification suite for smooth integration across all stages of the SoC design flow.

- **DoCD™ Hardware Debug System**
  Built-in support for **DoCD™**, DCD's real-time, non-intrusive hardware debugger, providing full visibility into CPU registers, SFRs, program and data memory, and user-defined peripherals—without disturbing real-time execution.

Ideal Applications

- Automotive electronics
- Battery-powered embedded systems
- Industrial controllers
- Legacy firmware migration to modern SoCs
- Long-lifecycle and safety-critical designs

The **D68HC11F IP Core** combines the reliability of the classic 68HC11F1 architecture with the flexibility, scalability, and integration advantages required by today's SoC designs—making it a future-proof solution for engineers who value compatibility without compromise.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND

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ASIC VENDORS.

For further details, email info@dcd-semi.com

CPU FEATURES

- Cycle compatible with original implementation
- Software compatible with 68HC11 industry standard
- I/O Wrapper making it pin-compatible core
- SFR registers remapped to any 4KB memory page
- Two power saving modes: STOP, WAI
- Fully synthesizable
- Static synchronous design
- No internal tri-states
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

PERIPHERALS

The peripherals listed below are implemented in a standard configuration of the D68HC11.

- **DoCD™ On-Chip Debugger**
  - Processor execution control
  - Read, write all processor contents
  - Hardware execution breakpoints
  - Three wire communication interface
- **I/O Ports**
- **Interrupt Controller**
  - Dedicated vector and interrupt priority for each interrupt source
- **Main 16-bit timer/counter system**
  - 16 bit free running counter
  - Four stage programmable prescaler
  - Real Time Interrupt
- **16-bit Compare/Capture Unit**
  - Three independent input-capture
  - Five output-compare channels
  - Events capturing
  - Pulses and digital signals generation
  - Gated timers
  - Sophisticated comparator
- **8-bit Pulse accumulator**
  - Two major modes of operation
  - Simple event counter
  - Gated time accumulation
  - Clocked by internal source or external pin
- **SPI – Master and Slave Serial Peripheral Interface**
  - Software selectable polarity and phase of serial clock SCK
  - System errors detection
  - Allows operation from a wide range of system clock frequencies (built-in 5-bit timer)
  - Interrupt generation
- **Full-duplex UART – SCI**
  - Standard non-return-to-zero format
  - 8 or 9 bit data transfer
  - Integrated baud rate generator
  - Noise, Overrun and Framing error detection
  - IDLE and BREAK characters generation
  - Wake-up block to recognize UART wake-up from IDLE condition
  - Three SCI related interrupts
- **Chip select unit**

OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented D68HC11F Microcontroller Core) are also available. The optional peripherals can be implemented upon customer's request.

- **PWM – Pulse Width Modulation Timer / Counter with up to four 8-bit or two 16-bit PWM channels**
- **I2C Master & Slave bus controllers**
  - Master operation
  - Multi-master systems supported
  - Performs arbitration and clock synchronization
  - Interrupt generation
  - Supports speed up to 3,4Mb/s (standard, fast & HS modes)
  - Allows operation from a wide range of clock frequencies (build-in 8-bit timer)
  - User-defined timing
- **Floating-Point Arithmetic Coprocessor (DFPAU) IEEE-754 standard single precision**
  - FADD, FSUB – addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM – compare
  - FCHS – change sign
  - FABS – absolute value
- **Floating-Point Math Coprocessor (DFPMU) – IEEE-754 standard single precision real, word and short integers**
  - FADD, FSUB- addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM- compare
  - FCHS – change sign
  - FABS – absolute value
  - FSIN, FCOS- sine, cosine
  - FPTAN, FPATAN- tangent, arcs tangent
- **Additional special internal interrupt dedicated for DFPAU or DFPMU**

UNITS SUMMARY

Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages execution of STOP instruction and waking the processor up from the STOP mode.
Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks**.**
ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index registers X, Y and related logic, like arithmetic unit, logic unit, multiplier and divider.
Bus Controller – Program Memory, Data Memory & SFR's (Special Function Register) interface – controls access into the

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program and data memories, and special registers. It contains Program Counter (PC), Stack Pointer (SP) register and related logic.

Interrupt Controller – D68HC11 extended IC has implemented 17-level interrupt priority control. The interrupt requests may come from external pins (IRQ and XIRQ), as well as from particular peripherals. The D68HC11 peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the CCR is cleared. Maskable interrupts are prioritized according to default arrangement, established during reset. However, any source may be elevated to the highest maskable priority position, by using HPRIO register. When interrupt condition occurs, an interrupt status flag is set, to indicate the condition.

Timer, Compare Capture & COP Watchdog – This timer system is based on a free-running, 16-bit counter with a 4-stage programmable prescaler. A timer overflow function allows software to extend the timing capability of the system, beyond the 16-bit range of the counter. Three independent input-capture functions are used, to automatically record the time, when a selected transition is detected at a respective timer input pin. Five output-compare functions are included, for generating output signals or for timing software delays. Since the input-capture and output-compare functions may not be familiar to all users, these concepts are explained in greater detail. A programmable periodic interrupt circuit, called RTI, is tapped off of the main 16-bit timer counter. Software can select one of four rates for the RTI, which is most commonly used to pace the execution of software routines. The COP watchdog function is loosely related to the main timer, in that the clock input to the COP system ($clk*2^{17}$) is tapped off the free-running counter chain. The timer subsystem involves more registers and control bits, than any other subsystem on the MCU. Each of the three input-capture functions has its own 16-bit time capture latch (input-capture register) and each of the five output-compare functions has its own 16-bit compare register. All timer functions, including the timer overflow and RTI, have their own interrupt controls and separate interrupt vectors. Additional control bits permit software to control the edge(s), that trigger each input-capture function and the automatic actions that result from output-compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is mainly a software-oriented system. This structure is easily adaptable to a very wide range of applications, although it is not as efficient, as a dedicated hardware for some specific timing applications.

SCI – The SCI is a full-duplex UART type asynchronous system, using standard non return to zero (NRZ) format: 1 start bit, 8 or 9 data bits and a 1 stop bit. The D68HC11E resynchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore, differences in baud rate between the sending device and the SCI are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time and majority logic decides the sense for the bit. The receiver also has the ability to enter a temporary standby mode (called receiver wakeup), to ignore messages intended for a different receiver. Logic automatically wakes the receiver up, in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multi-drop SCI networks. The SCI transmitter can produce queued characters of idle (whole characters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag, this SCI also provides a transmit complete (TC) indication, that can be used in applications with a modem.

SPI Unit – it's a fully configurable master/slave Serial Peripheral Interface, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications, in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols, to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates, for the serial clock. SPI automatically drives slave select outputs SSO[7:0] and address SPI slave device to exchange serially shifted data. Error-detection logic is included, to support interprocessor communications. A write-collision detector indicates, when an attempt is made to write data to the serial shift register, while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers, if more than one SPI devices simultaneously attempt to become bus master.

Pulse Accumulator – This system is based on an 8-bit counter and can be configured, to operate as a simple event counter or for gated time accumulation. Unlike the main timer, the 8-bit pulse accumulator counter can be read or written at any time (the 16-bit counter in the main timer cannot be written). Control bits allow the user to configure and control the pulse accumulator subsystem. Two maskable interrupts are associated with the system, each having its own controls and interrupt vector. The PAI pin associated with the pulse accumulator can be configured to act as a clock (event counting mode) or as a gate signal, to enable a free-running E divided by 64 clock to the 8-bit counter (gated time accumulation mode). The alternate functions of the pulse accumulator input (PAI) pin, present some interesting application possibilities.

I/O Ports – All ports are 8-bit general-purpose bi-directional I/O system. The PORTA, PORTB, PORTC, PORTD, PORTE, PORTF and PORTG data registers have their corresponding data direction registers DDRX to control ports data flow. It assures that all D68HC11's ports have full I/O selectable registers. Writes to any ports pins cause data to be stored in the data registers. If any port pins are configured as output then data registers are driven out of those pins. Reads from port pins configured as input causes that input pin is read. If port pins is configured as output, during read data register is read. Writes to any ports pins not configured as outputs, do not cause data to be driven out of those pins, but the data is stored in the output registers. Thus, if the pins later become outputs, the last data written to port will be driven out the port pins.

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ADCCTRL – External ADC Controller is used as an interface, between D68HC11 internal registers and external serial/parallel ADC converter. This module has several different options, so its details are described in separate document.
EEPROMCTRL – External Serial EEPROM controller. Manages data exchange between D68HC11 and external EEPROM. During initialization, copies contents of whole external EEPROM to internal EEPRAM (EEPROM Mirror implemented in standard parallel RAM). This module has several different options, so its details are described in separate document.
DoCD™ – Debug Unit – it's a real-time hardware debugger, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal, external, program memories, all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off. The separate CLKDOCD clock line allow the debugger to operate while the CPU is in STOP mode and the major clock line CLK is stopped.
Chip Select – Its role is to minimize the amount of external glue logic needed to interface the MCU to external devices.

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** devices (all key features included):

Technology	Optimization	Gates
0.25 typical	area	13 500

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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