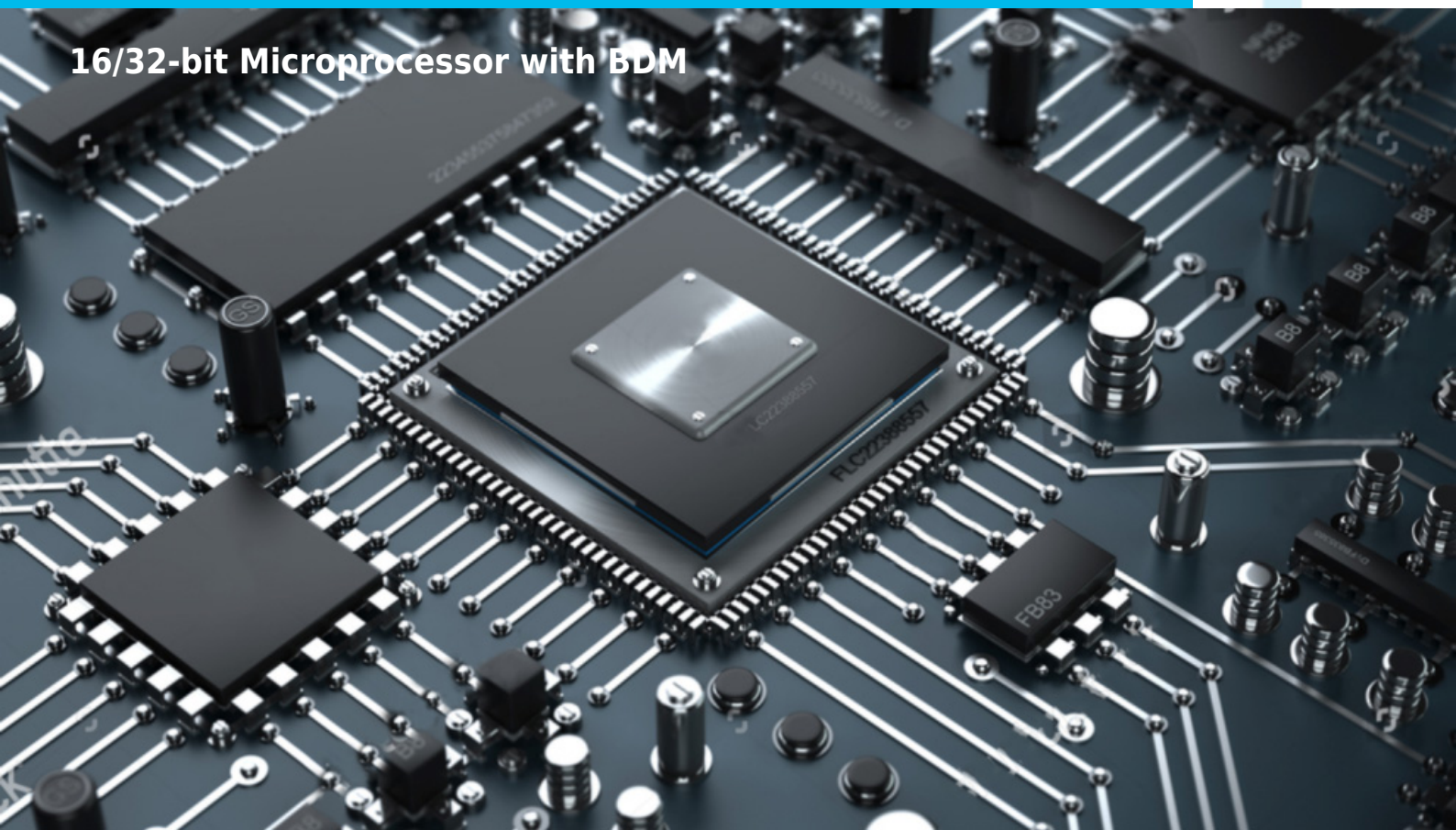
DIGITAL CORE DESIGN

D68000-BDM

16/32-bit Microprocessor with BDM



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The D68000-BDM soft core is binary-compatible with an industry-standard 68000 32-bit microprocessor. It has a 16-bit data bus and a 24-bit address data bus. Of course, the code is compatible with MC68008, upward compatible with MC68010 virtual extensions, and MC68020 32-bit implementation of the architecture. Our efficient IP Core has an improved instruction set, which allows the execution of the program with higher performance than a standard 68000 core. The D68000-BDM s delivered with a **fully automated test bench** and **complete set of tests**, allowing easy package validation at each stage of the SoC design flow. A special **testing platform** has been built to run **D68000-BDM with uCLinux** Operating System. The main goal of using uCLinux was to show that the D68000 microprocessor IP Core is fully functional and well validated. For that purpose, we have built a complete testing system based on CYCLONE-II DoCD2_C2_ETH_SDRAM32 FPGA board, with some onboard memories and peripherals. We have used the worldwide known Operating System for embedded solutions – **uCLinux,** to run with the D68000. Such a combination of hardware and software creates a **very useful and flexible platform** with the **D68000 IP Core as the main processor**. Most of the applications and tools were already available as GPL-based software. As a source for all information regarding uCLinux we have used http://www.uclinux.org/.

Watch the D68000-BDM presentation on DCD's You Tube:

As Seen On YouTube

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix***

CPU FEATURES

- Software compatible with 68000 industry standard
- **MULS, MULU** take **28 clock periods**
- **DIVS, DIVU** take **28 clock periods**
- Optimized shifts and rotations
- Idle cycles removed to improve performance
- Shorter effective address calculation time
- Bus cycle timings **identical to 68000**
- 32 bit data and address registers
- 14 addressing modes:
  - Direct:
    - Data register direct
    - Address register direct
  - Indirect:
    - Register indirect
    - Postincrement register indirect
    - Predecrement register indirect
    - Register indirect with offset
    - Indexed register indirect with offset
  - PC relative:
    - Relative with offset
    - Relative with index and offset
  - Absolute data:
    - Absolute short
    - Absolute long
  - Immediate data:
    - Immediate
    - Quick immediate
    - Implied
- 5 data types supported:
  - bits
  - BCD
  - bytes, words and long words
- Arithmetic Logic Unit includes:
  - 8,16,32-bit arithmetic & logical operations
  - 16×16 bit signed and unsigned multiplication
  - 32/16 bit signed and unsigned division
  - Boolean operations
- Interrupt controller:
  - 7 priority levels interrupt controller
  - Unlimited number of virtual interrupt sources
  - Vectored and auto-vectored modes
- Memory interface includes:
  - Up to 4 GB of address space
  - 16-bit data bus
  - Asynchronous bus control
- M6800 family synchronous interface
  - 3- and 2- wire bus arbitration
  - Supervisor and user modes
- Fully synthesizable
- Static synchronous design
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DOCD-BDM DEBUGGER

D68000 DoCD-BDM is a hardware debugger, which provides

debugging capability of a whole SoC system. Its main features are summarized below.

- **100% compatible with BDM debug interfaces**
- **Works with industry BDM interfaces/cables**
  - *Public Domain cable*
  - *Macraigor Wiggler*
  - *P&E BDM cable*
- **Full standard debugging tools support:**
  - *GNU GDB debugger*
  - *Cosmic ZAP debugger*
  - *Tasking debugger*

UNITS SUMMARY

ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator and related logic, such as arithmetic unit, logic unit, multiplier and divider. BCD operation are executed in this unit and condition code flags (N-negative, Z-zero, C-carry V-overflow) for most instructions.
Shifter – Performs shifting operations for the appropriate instructions, mainly for rotation, shift and bit operations.
Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions. Contains SR (status register is consisted of two portions: supervisor byte and user byte) and its related logic.
Opcode Decoder – Performs an instruction opcode decoding and the control functions for all blocks.
Memory Interface – Contains memory access related registers. It performs the memory addressing instructions code fetching and data transfers. It is responsible for all external bus cycle actions, such as: read & write, repeated read & write, halt and resume of bus cycles, bus arbitration provided by 3- and 2- wire system, correct bus and address errors handling, wait states cycle insertion and M6800 synchronous cycle generation.
Interrupt Controller – Interrupt Control module is responsible for the interrupt manage system for the external & internal interrupts and exceptions processing. It manages auto-vectored interrupt cycles, priority resolving and correct vector numbers creation.
Address registers – Contains 32-bit A0 to A6 address registers, two stack pointers USP (user SP) and SSP (Supervisor SP), 32-bit Program counter and related logic to perform word and long address operations. Effective address operations are executed in this unit.
Data registers – Contains 32-bit data registers D0 to D7 and related logic to perform byte, word and long data operations.
DoCD-DBM – a hardware debugger which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, DoCD-BDM provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, patch user code, read/write any contents of microprocessor including all registers, memories and user connected peripherals. Hardware breakpoints can be set and controlled on program and data memories. One additional pin FREEZE indicates the state of the CPU. It is active when the CPU is halted and the debugger is in action. The DoCD-BDM system includes **SPI-like serial interface** and complete set of tools, to communicate and work with core in a real time debugging. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

PERFORMANCE

The following table gives a survey about the Core area and performance in **INTEL FPGA®** devices after Place & Route (all key features included):

Device	Speed grade	LE/ALM	F_{max}
APEX20KE	-1	6 332	32 MHz
APEX20KC	-7	6 332	37 MHz
APEX-II	-7	6 657	40 MHz
MERCURY	-5	7 086	45 MHz
STRATIX	-5	6 862	49 MHz
CYCLONE	-6	6 604	44 MHz

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed

product can be used at selected company branches.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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