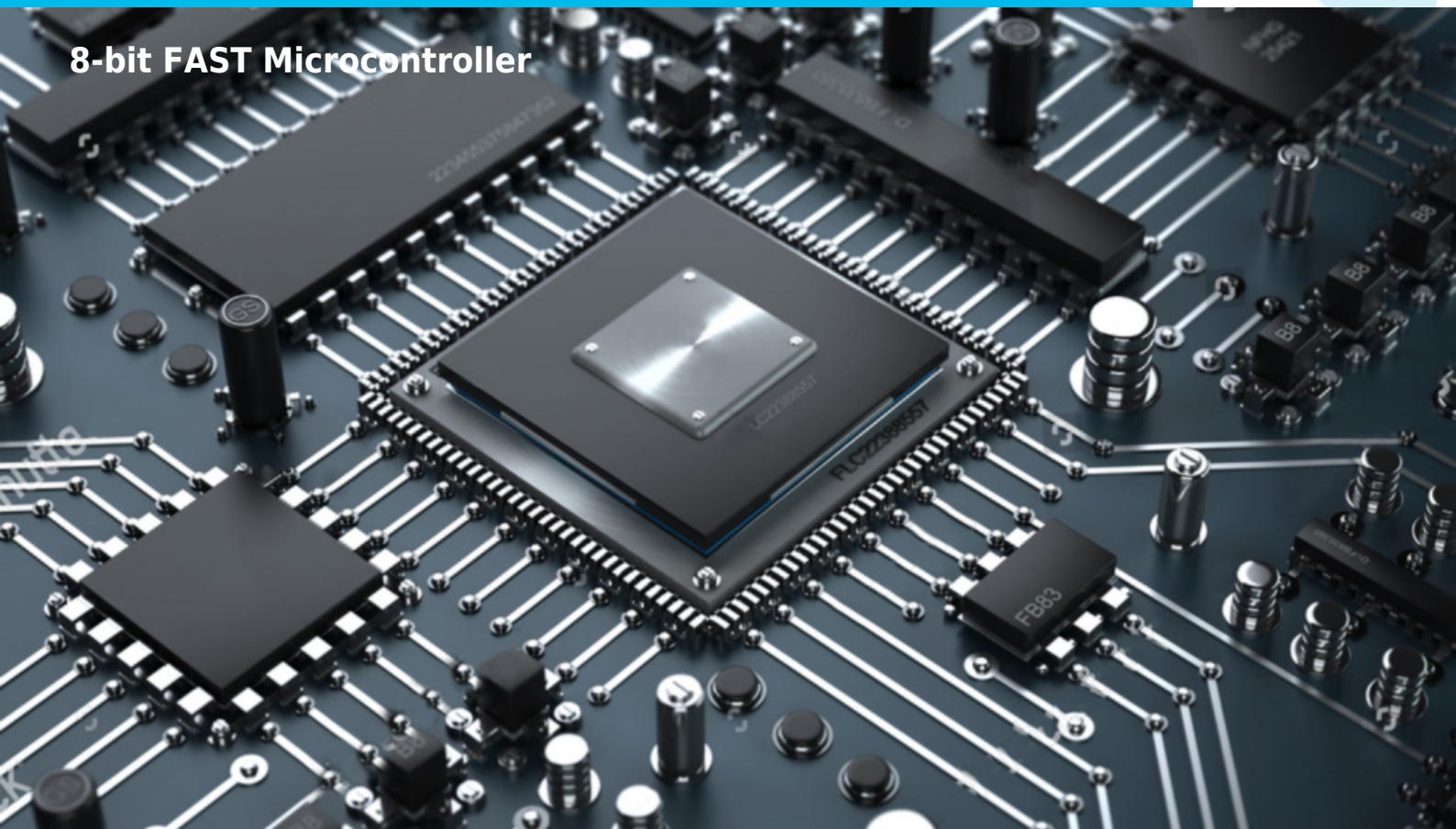


DF6811E



8-bit FAST Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The **DF6811** is an advanced 8-bit MCU IP Core with highly sophisticated, on-chip peripheral capabilities. The IP Core is **binary-compatible with industry-standard Motorola 68HC11 8-bit microcontroller**. It has an **improved FAST architecture** which is approximately **4 times faster** compared to the original implementation. In the standard configuration, the core has major peripheral functions integrated on-chip. It can be provided in configurations that match the following specs:

- **68HC11A**
- **68HC11D**
- **68HC11E**

There are two serial interfaces: an asynchronous serial communications interface (SCI) and a separate synchronous serial peripheral interface (SPI). The main 16-bit, free-running timer system has three input capture lines, five output-compare lines, and a real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods. Self-monitoring circuitry is included on-chip to protect against system errors. The Computer Operating Properly (COP) watchdog system protects against software failures. An illegal opcode detection circuit provides a non-maskable interrupt if an illegal opcode is detected. Two software-controlled **power-saving modes** - WAIT and STOP are available to save additional power. These modes make the DF6811 IP Core especially attractive for **automotive and battery-driven applications**. The DF6811E Microcontroller Core can be equipped with **ADC Controller, allowing the use of an external ADC Controller with standard ADC software. The ADC Controller makes external ADCs visible as internal ADCs in original 68HC11E Microcontrollers**. The DF6811E is fully customizable - delivered in the exact configuration to meet your requirements. There is no need to pay extra for unused features and wasted silicon. The DF6811E comes with a **fully automated test bench** and a **complete set of tests**, allowing easy package validation at each stage of SoC design flow. Each DCD's DF68XX Core has built-in support for a proprietary Hardware Debug System called **DoCD™** - a **real-time hardware debugger** providing the debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** allows **non-intrusive**

debugging of a running application. It can halt, run, step into or skip an instruction, and read/write any contents of the microcontroller, including all registers, and SFRs, including user-defined peripherals, data, and program memories.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- **Altera / Intel,**
- **Xilinx / AMD,**
- **Lattice,**
- **Microsemi / Microchip,**
and others.
- **TSMC**
- **UMC**
- **SK Hynix**
and others.

CPU FEATURES

- FAST architecture, **4 times faster** than the original implementation
- Software compatible with industry standard 68HC11
- 10 times faster multiplication
- 16 times faster division
- 256 bytes of remapped System Function Registers space (SFRs)
- De-multiplexed Address/Data Bus, to allow easy memory connection
- **Core can also be used without I/O wrapper, so each peripheral functions pins will be separated from I/O ports lines.**
- Two power saving modes: STOP, WAIT
- Ready pin allows Core to operate with slow program and data memories.
- Fully synthesizable
- Static synchronous design
- No internal reset generator or gated clock
- Positive edge clocking and no internal tri-states
- Scan test ready
- **1 GHz** of virtual clock frequency compared to original implementation
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

PERIPHERALS

The peripherals listed below are implemented in the standard configuration of DF6811E.

- **DoCD™ On-Chip Debugger**
 - Processor execution control
 - Read, write all processor contents
 - Hardware execution breakpoints
 - Three wire communication interface
- **I/O Ports**
- **Interrupt Controller**
 - Dedicated vector and interrupt priority for each

interrupt source

- **Main 16-bit timer/counter system**
 - 16 bit free running counter
 - Four stage programmable prescaler
 - Real Time Interrupt
- **16-bit Compare/Capture Unit**
 - Three independent input-capture
 - Five output-compare channels
 - Events capturing
 - Pulses and digital signals generation
 - Gated timers
 - Sophisticated comparator
 - Pulse width modulation and measuring
- **8-bit Pulse accumulator**
 - Two major modes of operation
 - Simple event counter
 - Gated time accumulation
 - Clocked by internal source or external pin
- **SPI - Master and Slave Serial Peripheral Interface**
 - Software selectable polarity and phase of serial clock SCK
 - System errors detection
 - Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)
 - Interrupt generation
- **Full-duplex UART - SCI**
 - Standard non-return-to-zero format
 - 8 or 9 bit data transfer
 - Integrated baud rate generator
 - Noise, Overrun and Framing error detection
 - IDLE and BREAK characters generation
 - Wake-up block to recognize UART wake-up from IDLE condition
 - Three SCI related interrupts

OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented DF6811E Microcontroller Core) can be implemented upon customer's request.

- **PWM - Pulse Width Modulation Timer/Counter with up to four 8-bit or two 16-bit PWM channels**
- **Memory extension unit and Chip select**
- **I2C Master & Slave bus controllers**
 - Master operation
 - Multi-master systems supported
 - Performs arbitration and clock synchronization
 - Interrupt generation
 - Supports speed up to 3,4Mb/s (standard, fast & HS modes)
 - Allows operation from a wide range of clock frequencies (build-in 8-bit timer)
 - User-defined timing
- **Floating-Point Arithmetic Coprocessor (DFPAU) IEEE-754 standard single precision**
 - FADD, FSUB - addition, subtraction
 - FMUL, FDIV- multiplication, division
 - FSQRT- square root
 - FUCOM - compare

- FCHS - change sign
- FABS - absolute value
- **Floating-Point Math Coprocessor (DFPMU) - IEEE-754 standard single precision real, word and short integers**
 - FADD, FSUB- addition, subtraction
 - FMUL, FDIV- multiplication, division
 - FSQRT- square root
 - FUCOM- compare
 - FCHS - change sign
 - FABS - absolute value
 - FSIN, FCOS- sine, cosine
 - FPTAN, FPATAN- tangent, arcs tangent
 - Additional special internal interrupt dedicated for DFPAU or DFPMU

UNITS SUMMARY

Control Unit - Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages execution of STOP instruction and wakes the processor up from the STOP mode.

Opcode Decoder - Performs an instruction opcode decoding and the control functions for all other blocks.

ALU - Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (A), Condition Code Register (CCREG), Index registers (X) and related logic like arithmetic unit, logic unit and multiplier.

Bus Controller - Program Memory, Data Memory & SFR's (Special Function Register) interface - controls access into the program and data memories and special registers. It contains Program Counter (PC), Stack Pointer (SP) register and related logic.

Interrupt Controller - Extended IC has implemented 7-level interrupt priority control. The interrupt requests may come from external pin (IRQ), as well as from particular peripherals. The DF6805 peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the CCR is cleared. Maskable interrupts are prioritized, according to default arrangement established during reset. When interrupt condition occurs, an interrupt status flag is set, to indicate the condition.

Timer & Compare - The programmable timer is based on free-running 16-bit counter, with a fixed divide by four prescaler, plus input capture/output compare circuitry. The timer can be used for many purposes, including measuring pulse length of two input signals and generating two output signals. The timer has 16-bit architecture hence each specific functional segment is represented by two 8-bit registers. These registers contain the high and low byte of that functional block. Accessing the low byte of a specific timer function, allows full control of that function, however, an access of the high byte inhibits that specific timer function, until the byte is also accessed. Each of the input-capture channel has its own 16-bit time capture latch (input-capture register) and each of the output-compare channel, has its own 16-bit compare register. Additional control bits permit software to control the edge(s), that trigger each input-capture function and the automatic actions that result from

output-compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is mainly a software-oriented system. This structure is easily adaptable to a very wide range of applications, although for some specific timing applications, it is not as efficient, as a dedicated hardware.

SCI - The SCI is a full-duplex UART type, asynchronous system, using standard non return to zero (NRZ) format: 1 start bit, 8 or 9 data bits and a 1 stop bit. The DF6805 resynchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore, differences in baud rate, between the sending device and the SCI, are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time and majority logic decides the sense for the bit. For the start and stop bits, seven logic samples are taken. Even if noise causes one of these samples to be incorrect, the bit will still be received correctly. The receiver also has the ability, to enter a temporary standby mode (called receiver wakeup), to ignore messages intended for a different receiver. Logic automatically wakes the receiver up, in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multi-drop SCI networks. The SCI transmitter can produce queued characters of idle (whole characters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag, this SCI also provides a transmit complete (TC) indication, that can be used in applications with a modem.

SPI Unit - it's a fully configurable master/slave Serial Peripheral Interface, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller, to communicate with serial peripheral devices. It is also capable of interprocessor communications, in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information, on the two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough, to interface directly with numerous standard product peripherals, from several manufacturers. Data rates are as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols, to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock. SPI automatically drives slave select outputs SSO[7:0] and address SPI slave device, to exchange serially shifted data. Error-detection logic is included, to support interprocessor communications. A write-collision detector indicates, when an attempt is made to write data to the serial shift register, while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers, if more than one SPI devices, simultaneously attempt to become a bus master.

Pulse Accumulator - This system is based on an 8-bit counter and can be configured, to operate as a simple event counter or for gated time accumulation. Unlike the main timer, the 8-bit pulse accumulator counter can be read or written at any time (the 16-bit counter in the main timer cannot be written). Control bits allow the user, to configure and control the pulse accumulator subsystem. Two maskable interrupts are associated with the system, each having its

own controls and interrupt vector. The PAI pin associated with the pulse accumulator can be configured to act as a clock (event counting mode) or as a gate signal, to enable a free-running E divided by 64 clock to the 8-bit counter (gated time accumulation mode). The alternate functions of the pulse accumulator input (PAI) pin, present some interesting application possibilities.

I/O Ports - All ports are 8-bit general-purpose bi-directional I/O system. The PORTA, PORTB, PORTC, PORTD data registers have their corresponding data direction registers DDRA, DDRB, DDRC, DDRD, to control ports data flow. It assures, that all DF6808's ports have full I/O selectable registers. Writes to any ports pins cause data to be stored in the data registers. If any port pins are configured as output, then data registers are driven out of those pins. Reads from port pins configured as input, causes that input pin is read. If port pins is configured as output, during read data register is read. Writes to any ports pins, not configured as outputs, do not cause data to be driven out of those pins, but the data is stored in the output registers. Thus, if the pins later become outputs, the last data written to port will be driven out the port pins.

ADCCTRL - External ADC Controller, used as an interface between DF6811 internal registers and external serial/parallel ADC converter. This module has several different options, so its details are described in a separate document.

EEPROMCTRL - External Serial EEPROM controller. Manages data exchange between D68HC11E and external EEPROM. During initialization, copies contents of whole external EEPROM, to internal EEPROM (EEPROM Mirror implemented in standard parallel RAM). This module has several different options, so its details are described in separate document.

DoCD™ - a real-time hardware debugger which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal, external, program memories, all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off. The separate CLKDOCD clock line allows the debugger to operate, while the CPU is in STOP mode and the major clock line CLK is stopped.

DESIGN FEATURES

- One global system clock
- Synchronous reset
- All asynchronous input signals are synchronized before internal use

PERFORMANCE

To provide you with the most accurate and detailed insights about the Intel performance, we encourage you to get in touch with us directly.

Please feel free to contact us at info@dcd.pl. Our dedicated team will be more than happy to assist you with any inquiries you may have.

DELIVERABLES

- Source code:
 - VERILOG or VHDL Source Code
 - VERILOG or VHDL test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
 - Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
 - Synthesis scripts
 - Example application
- Netlist
 - Netlist for selected FPGA family
 - Sample FPGA project
 - Technical documentation
 - HDL core specification
 - Datasheet
- Technical support
 - IP Core implementation
 - 12 months maintenance
 - Delivery of the IP Core and documentation updates

- Phone & email support
- Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

- **Single-Site license option** - dedicated to small and middle sized companies which run their business at one place.

- **Multi-Site license option** - dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:

- VHDL or Verilog RTL synthesizable source code (called HDL Source code)

- FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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