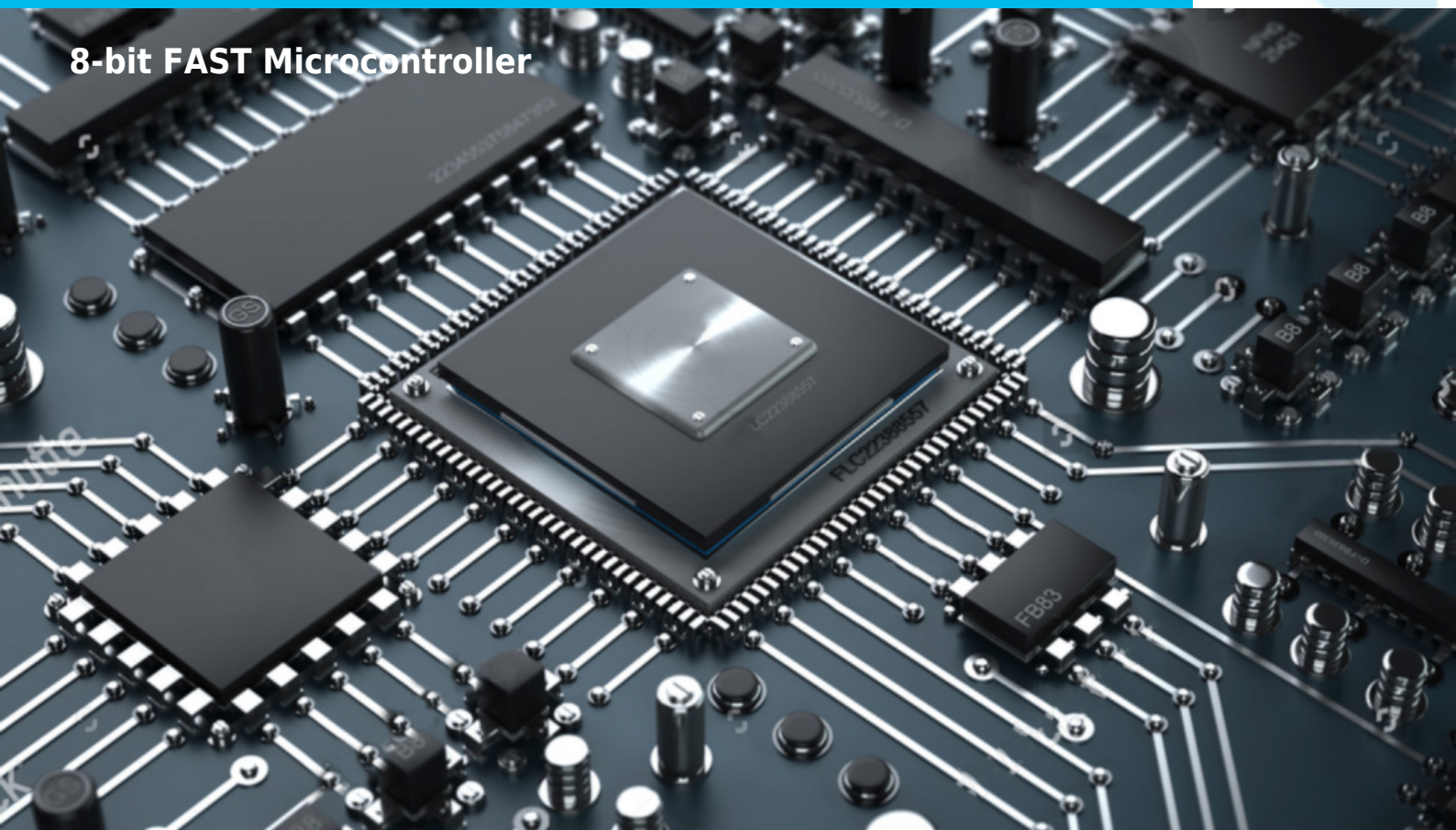
DIGITAL CORE DESIGN

DF6811F

8-bit FAST Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DF6811F – HIGH-PERFORMANCE 68HC11F-COMPATIBLE 8-BIT MCU IP CORE

The **DF6811F** is a **high-performance, 8-bit microcontroller IP Core**, fully **binary-compatible with the industry-standard Motorola 68HC11F** MCU. Designed as a modern drop-in replacement for legacy 68HC11F devices, DF6811F enables **seamless migration of existing software** while delivering **significantly higher performance, lower power consumption, and full SoC-level customization**.

At the heart of DF6811F is DCD-SEMI's **FAST CPU architecture**, delivering **up to 4× higher performance** compared to the original 68HC11F implementation. This allows designers to achieve higher throughput at lower clock frequencies, resulting in **improved efficiency and reduced power consumption**.

Key Features of DF6811F IP Core

- **100% binary compatibility** with Motorola 68HC11F
- **Up to 4× performance improvement** with FAST architecture
- **Integrated on-chip peripherals** in standard configuration
- **FPGA and ASIC-ready soft IP Core**
- **Long-term availability** for industrial and automotive designs

Integrated Peripherals and Interfaces

The DF6811F includes a rich set of **on-chip peripherals**, matching and extending the original 68HC11F functionality:

- **Two serial interfaces**
  - Asynchronous Serial Communication Interface (**SCI**)
  - Synchronous Serial Peripheral Interface (**SPI**)
- **Advanced 16-bit free-running timer system**
  - 3 input capture lines
  - 5 output compare channels
  - Real-Time Interrupt (RTI) support
- **8-bit pulse accumulator**
  - Counts external events
  - Measures external signal periods

Reliability, Safety, and Power Management

DF6811F integrates multiple hardware mechanisms to ensure **robust operation in safety-critical environments**:

- **Computer Operating Properly (COP) watchdog** for software fault detection
- **Illegal opcode detection** generating a non-maskable interrupt (NMI)
- **Self-monitoring circuitry** to protect against system errors

For power-sensitive designs, DF6811F supports **two software-controlled low-power modes**:

- **WAIT mode**
- **STOP mode**

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These features make the DF6811F an excellent choice for **automotive, industrial, and battery-powered applications**.

External ADC Support with Software Transparency

The **DF6811F Microcontroller Core** can be equipped with an **ADC Controller**, enabling seamless integration of an **external ADC** while maintaining **full software compatibility** with original 68HC11F ADC firmware. External ADCs appear to software as **internal ADC peripherals**, eliminating the need for code modifications.

Fully Customizable Soft IP – No Wasted Silicon

The DF6811F is delivered in an **exact, application-specific configuration**, allowing designers to include only the required features:

- No unused peripherals
- No unnecessary logic
- Optimized silicon area and cost

This **pay-only-for-what-you-use model** makes DF6811F ideal for both high-volume and specialized designs.

Advanced Debug with DoCD™ Hardware Debug System

Each DF6811F Core includes built-in support for **DoCD™**, DCD-SEMI's **non-intrusive, real-time hardware debug system**. DoCD™ enables full visibility and control of the entire System-on-Chip:

- Halt, run, step into, or skip instructions
- Read/write all registers and SFRs
- Debug user-defined peripherals
- Access program and data memory in real time

Unlike traditional on-chip debuggers, **DoCD™ does not disturb the running application**, making it ideal for real-time and safety-critical systems.

Why Choose DF6811F?

> **DF6811F is the fastest, safest, and lowest-risk way to modernize 68HC11F-based designs—without rewriting a single line of code.**

DF6811F vs Original 68HC11F comparison table:

Feature	DF6811F IP Core	Original 68HC11F
CPU Architecture	FAST 8-bit MCU, 4× faster than original	Standard 8-bit MCU
Binary Compatibility	100% compatible with 68HC11F	Native
Program & Data Bus	Configurable, ASIC/FPGA ready	Fixed 16-bit program, 8-bit data bus
Integrated Peripherals	SCI, SPI, 16-bit timers, pulse accumulator, ADC support	SCI, SPI, 16-bit timers, pulse accumulator
Performance	Up to 4× faster execution, optimized instruction set	Baseline performance of original MCU
Low-Power Modes	WAIT and STOP modes for battery-powered designs	Limited low-power functionality
Error Protection	COP watchdog, illegal opcode detection, self-monitoring circuitry	COP watchdog (basic)
Debugging	Built-in DoCD™ non-intrusive hardware debugger	No advanced on-chip debugger
Customization	Fully configurable for SoC, ASIC, or FPGA, no wasted logic	Fixed design, not customizable
External ADC Support	Optional ADC Controller with software transparency	ADC integrated, no external extension support
SoC Integration	Ready for multi-channel FPGA/ASIC integration	Limited

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

CPU FEATURES

- FAST architecture, **4 times faster** than the original implementation
- Software compatible with 68HC11 industry standard
- 10 times faster multiplication
- 16 times faster division
- 256 bytes of remapped System Function Registers space (SFRs)
- De-multiplexed Address/Data Bus, to allow easy memory connection
- **Core can also be used without I/O wrapper, so each peripheral functions pins will be separated from I/O ports lines.**
- Two power saving modes: STOP, WAI
- Ready pin allows Core to operate with slow program and

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data memories.
- Fully synthesizable
- Static synchronous design
- No internal reset generator or gated clock
- Positive edge clocking and no internal tri-states
- Scan test ready
- **1 GHz** of virtual clock frequency compared to the original implementation
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

- One global system clock
- Synchronous reset
- All asynchronous input signals are synchronized before internal use

PERIPHERALS

The peripherals listed below are implemented in the standard configuration of DF6811F.

- **DoCD™ On-Chip Debugger**
  - Processor execution control
  - Read, write all processor contents
  - Hardware execution breakpoints
  - Three wire communication interface
- **I/O Ports**
- **Interrupt Controller**
  - Dedicated vector and interrupt priority for each interrupt source
- **Main16-bit timer/counter system**
  - 16 bit free running counter
  - Four stage programmable prescaler
  - Real Time Interrupt
- **16-bit Compare/Capture Unit**
  - Three independent input-capture
  - Five output-compare channels
  - Events capturing
  - Pulses and digital signals generation
  - Gated timers
  - Sophisticated comparator
  - Pulse width modulation and measuring
- **8-bit Pulse accumulator**
  - Two major modes of operation
  - Simple event counter
  - Gated time accumulation
  - Clocked by internal source or external pin
- **SPI – Master and Slave Serial Peripheral Interface**
  - Software selectable polarity and phase of serial clock SCK
  - System errors detection
  - Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)
  - Interrupt generation
- **Chip Select Unit**
- **Full-duplex UART – SCI**
  - Standard Non-return to Zero format
  - 8 or 9 bit data transfer
  - Integrated baud rate generator
  - Noise, Overrun and Framing error detection
  - IDLE and BREAK characters generation
  - Wake-up block to recognize UART wake-up from IDLE condition
  - Three SCI related interrupts

OPTIONAL PERIPHERALS

Optional peripherals (not included in the presented DF6811F Microcontroller Core) can be implemented upon customer's request.

- **PWM – Pulse Width Modulation Timer/Counter with up to four 8-bit or two 16-bit PWM channels**
- **Memory extension unit and Chip select**
- **I2C Master & Slave bus controllers**
  - Master operation
  - Multi-master systems supported
  - Performs arbitration and clock synchronization
  - Interrupt generation
  - Supports speed up to 3,4Mb/s (standard, fast & HS modes)
  - Allows operation from a wide range of clock frequencies (build-in 8-bit timer)
  - User-defined timing
- **Floating-Point Arithmetic Coprocessor (DFPAU) IEEE-754 standard single precision**
  - FADD, FSUB – addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM – compare
  - FCHS – change sign
  - FABS – absolute value
- **Floating-Point Math Coprocessor (DFPMU) – IEEE-754 standard single precision real, word and short integers**
  - FADD, FSUB- addition, subtraction
  - FMUL, FDIV- multiplication, division
  - FSQRT- square root
  - FUCOM- compare
  - FCHS – change sign
  - FABS – absolute value
  - FSIN, FCOS- sine, cosine
  - FPTAN, FPATAN- tangent, arcs tangent
  - Additional special internal interrupt dedicated for DFPAU or DFPMU

UNITS SUMMARY

Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages execution of STOP instruction and wakes the processor up from the STOP mode.
Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks**.**
ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (A), Condition Code Register (CCREG), Index registers (X) and related logic like arithmetic unit, logic unit

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and multiplier.

Bus Controller – Program Memory, Data Memory & SFR's (Special Function Register) interface – controls access into the program and data memories and special registers. It contains Program Counter (PC), Stack Pointer (SP) register and related logic.

Interrupt Controller – extended IC has implemented 7-level interrupt priority control. The interrupt requests may come from external pin (IRQ), as well as from particular peripherals. The DF6805 peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the CCR is cleared. Maskable interrupts are prioritized, according to default arrangement established during reset. When interrupt condition occurs, an interrupt status flag is set, to indicate the condition.

Timer & Compare – The programmable timer is based on free-running 16-bit counter, with a fixed divide by four prescaler, plus input capture/output compare circuitry. The timer can be used for many purposes, including measuring pulse length of two input signals and generating two output signals. The timer has 16-bit architecture hence each specific functional segment is represented by two 8-bit registers. These registers contain the high and low byte of that functional block. Accessing the low byte of a specific timer function, allows full control of that function, however, an access of the high byte inhibits that specific timer function, until the byte is also accessed. Each of the input-capture channel has its own 16-bit time capture latch (input-capture register) and each of the output-compare channel, has its own 16-bit compare register. Additional control bits permit software to control the edge(s), that trigger each input-capture function and the automatic actions that result from output-compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is mainly a software-oriented system. This structure is easily adaptable to a very wide range of applications, although for some specific timing applications, it is not as efficient, as a dedicated hardware.

SCI – The SCI is a full-duplex UART type, asynchronous system, using standard non return to zero (NRZ) format: 1 start bit, 8 or 9 data bits and a 1 stop bit. The DF6805 resynchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore, differences in baud rate, between the sending device and the SCI, are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time and majority logic decides the sense for the bit. For the start and stop bits, seven logic samples are taken. Even if noise causes one of these samples to be incorrect, the bit will still be received correctly. The receiver also has the ability, to enter a temporary standby mode (called receiver wakeup), to ignore messages intended for a different receiver. Logic automatically wakes the receiver up, in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multi-drop SCI networks. The SCI transmitter can produce queued characters of idle (whole characters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag, this SCI also provides a transmit complete (TC) indication, that can be used in applications with a modem.

SPI Unit – it's a fully configurable master/slave Serial Peripheral Interface, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller, to communicate with serial peripheral devices. It is also capable of interprocessor communications, in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information, on the two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough, to interface directly with numerous standard product peripherals, from several manufacturers. Data rates are as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols, to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock. SPI automatically drives slave select outputs SSO[7:0] and address SPI slave device, to exchange serially shifted data. Error-detection logic is included, to support interprocessor communications. A write-collision detector indicates, when an attempt is made to write data to the serial shift register, while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers, if more than one SPI devices, simultaneously attempt to become a bus master.

Pulse Accumulator – This system is based on an 8-bit counter and can be configured, to operate as a simple event counter or for gated time accumulation. Unlike the main timer, the 8-bit pulse accumulator counter can be read or written at any time (the 16-bit counter in the main timer cannot be written). Control bits allow the user, to configure and control the pulse accumulator subsystem. Two maskable interrupts are associated with the system, each having its own controls and interrupt vector. The PAI pin associated with the pulse accumulator can be configured to act as a clock (event counting mode) or as a gate signal, to enable a free-running E divided by 64 clock to the 8-bit counter (gated time accumulation mode). The alternate functions of the pulse accumulator input (PAI) pin, present some interesting application possibilities.

I/O Ports – All ports are 8-bit general-purpose bi-directional I/O system. The PORTA, PORTB, PORTC, PORTD data registers have their corresponding data direction registers DDRA, DDRC, DDRD to control ports data flow. It assures that all DF6811's ports have full I/O selectable registers. Writes to any ports pins cause data to be stored in the data registers. If any port pins are configured as output, then data registers are driven out of those pins. Reads from port pins configured as input, causes that input pin is read. If port pins is configured as output, during read data register is read. Writes to any ports pins, not configured as outputs, do not cause data to be driven out of those pins, but the data is stored in the output registers. Thus, if the pins later become outputs, the last data written to port will be driven out the port pins.

ADCCTRL – External ADC Controller, used as an interface between DF6811 internal registers and external serial/parallel ADC converter. This module has several different options, so its details are described in a separate document.

EEPROMCTRL – External Serial EEPROM controller. Manages data exchange between D68HC11E and external EEPROM. During initialization copy contents of whole external EEPROM

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to internal EEPRAM (EEPROM Mirror implemented in standard parallel RAM). This module has several different options, so its details are described in separate document.
DoCD™ – a real-time hardware debugger which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal, external, program memories, all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurs at particular address, with certain data pattern or without pattern. **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off. The separate CLKDOCD clock line allows the debugger to operate, while the CPU is in STOP mode and the major clock line CLK is stopped.
CHIP SELECT – The function of the chip select is, to minimize the amount of external glue logic, needed to interface the MCU to external devices. Four software configured chip selects that can be enabled in expanded modes. The chip selects for I/O (CSIO1 and CSIO2) are used for I/O expansion. The program chip select (CSPROG) is used with an external memory, that contains the program code and reset vectors. The general-purpose chip select (CSGEN), is the most flexible and is used to enable external devices.

PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** devices (all key features included):

Technology	Optimization	Gates
0.25 typical	area	14 000

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.
– Remote Access license option – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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