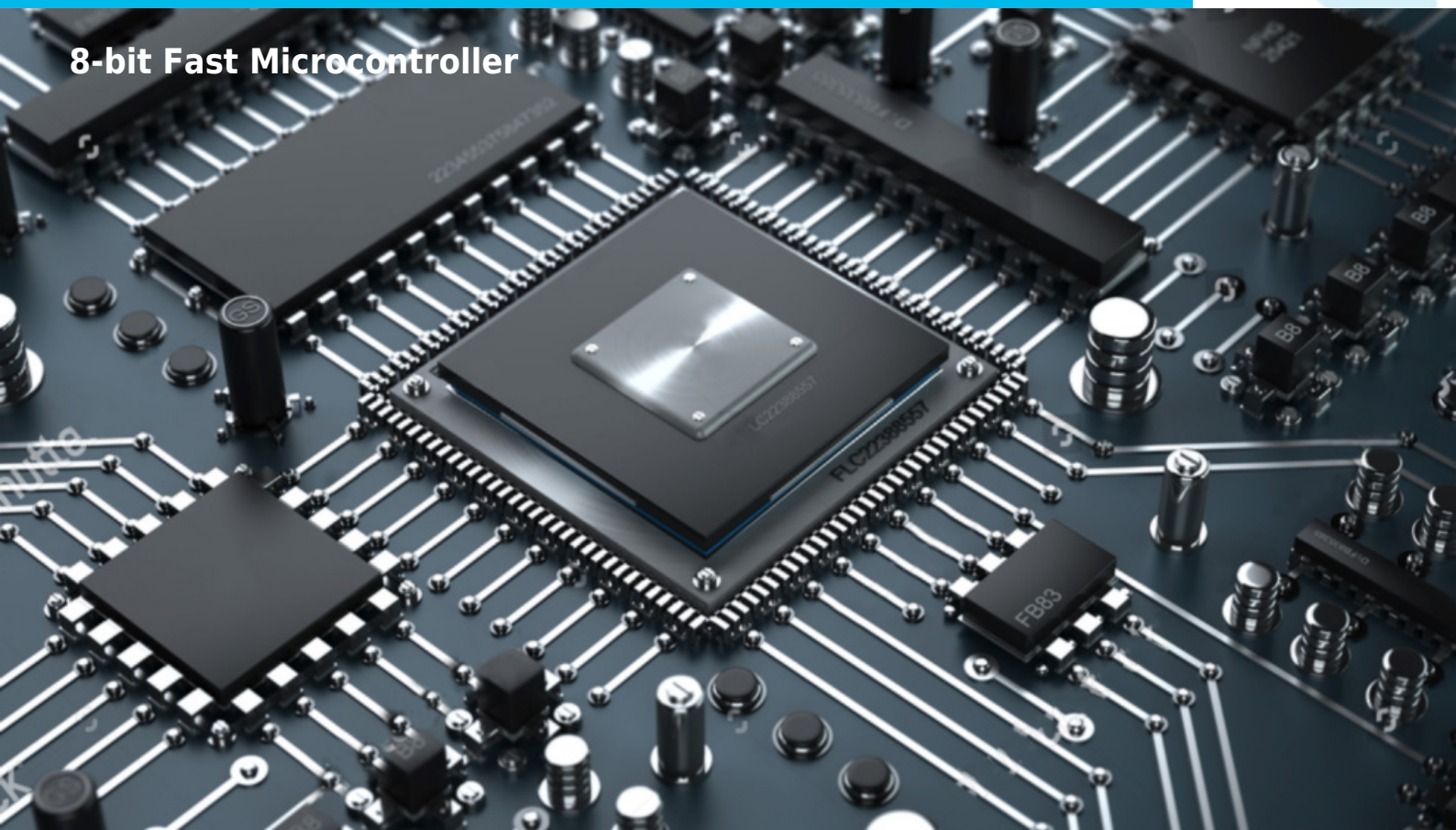
DIGITAL CORE DESIGN

DF6803



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DF6803 8-bit Soft MCU IP Core – High-Performance, Fully Configurable MC6803-Compatible

The **DF6803** is a high-performance, synthesizable 8-bit microcontroller IP Core, fully compatible with the industry-standard Motorola MC6803. Leveraging **DCD's enhanced internal architecture**, the DF6803 executes code up to **4× faster** than the original MC6803 at the same clock frequency, making it perfect for **automotive, industrial, and battery-powered SoC applications**.

Key Features & Capabilities:

- **Full MC6803 Compatibility:** Runs existing MC6803 code seamlessly, enabling easy migration.
- **Enhanced Architecture:** Delivers superior performance while maintaining full compatibility.
- **Customization:** Fully configurable to meet your project requirements, reducing unused features and wasted silicon.
- **Test Bench & Verification:** Delivered with a **fully automated test bench** and complete set of tests for easy SoC validation.
- **DoCD™ Hardware Debug:** Built-in **real-time, non-intrusive debugger**, allowing halt, run, step into/over instructions, and read/write access to all registers, SFRs, user-defined peripherals, and program/data memory.
- **Power Efficiency:** Supports low-power designs, suitable for embedded, battery-driven systems.

Ideal Applications: Automotive electronics, industrial SoCs, battery-powered embedded systems, and high-performance 8-bit microcontroller projects.

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

CPU FEATURES

- **Improved, 4 times faster architecture**
- **Software compatible with industry standard MC6803**
- I/O Wrapper making it pin compatible core
- Power saving mode: WAI
- Fully synthesizable
- Static synchronous design
- No internal tri-states
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

UNITS SUMMARY

SCI – a full-duplex UART type asynchronous system using standard non return to zero (NRZ) format: 1 start bit and stop bit. The Core re-synchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore differences in baud rate between the sending device and the SCI are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time and majority logic decides the sense for the bit. For the start and stop bits seven logic samples are taken. Even if noise causes one of these samples to be incorrect, the bit will still be received correctly. The receiver also has the ability to enter a temporary standby mode (called receiver wakeup) to ignore messages intended for a different receiver. Logic automatically wakes up the receiver in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multidrop SCI networks. The SCI transmitter can produce queued characters of idle (whole characters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag.
I/O Ports – General Purpose I/O Ports. When enabled, the I/O Ports are shared with particular on chip peripherals: SCI and TIMER.
Timer with Compare Capture – The programmable timer is based on a free-running 16-bit counter and input capture/output compare circuitry. The timer can be used for many purposes, including measuring pulse length of two input signals and generating two output signals. The timer has a 16-bit architecture, hence each specific functional segment is represented by two 8-bit registers. These registers contain the high and the low byte of that functional block. Accessing the low byte of a specific timer function, allows full control of that function, however, an access of the high byte, inhibits that specific timer function, until the byte is also accessed.
Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks.
Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages HALT input pin

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events.
Interrupt Controller – Responsible for the interrupt manage system, for the processing of the external and internal interrupts and exceptions. It manages auto-vectored interrupt cycles, priority resolving and correct vector numbers creation.
DoCD™ Debug Unit – **real-time hardware debugger**, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal and external program memories, all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when the debug option is no longer used, the whole debugger is turned off. The separate **DoCD™** clock line allows debugger to operate in the SLEEP mode (major clock line CLK is stopped).
Bus Controller – Program Memory, Data Memory interface, controls access into the program and data memories. It contains Program Counter (PC), Stack Pointer (SP) register, and related logic.
ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index register X and related logic, like arithmetic unit, logic unit, multiplier and divider.

PERFORMANCE

For precise **LATTICE FPGA** performance insights, reach out to us at info@dcd.pl. Our dedicated team is ready to assist you with any inquiries.

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Remote Access license option* – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

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