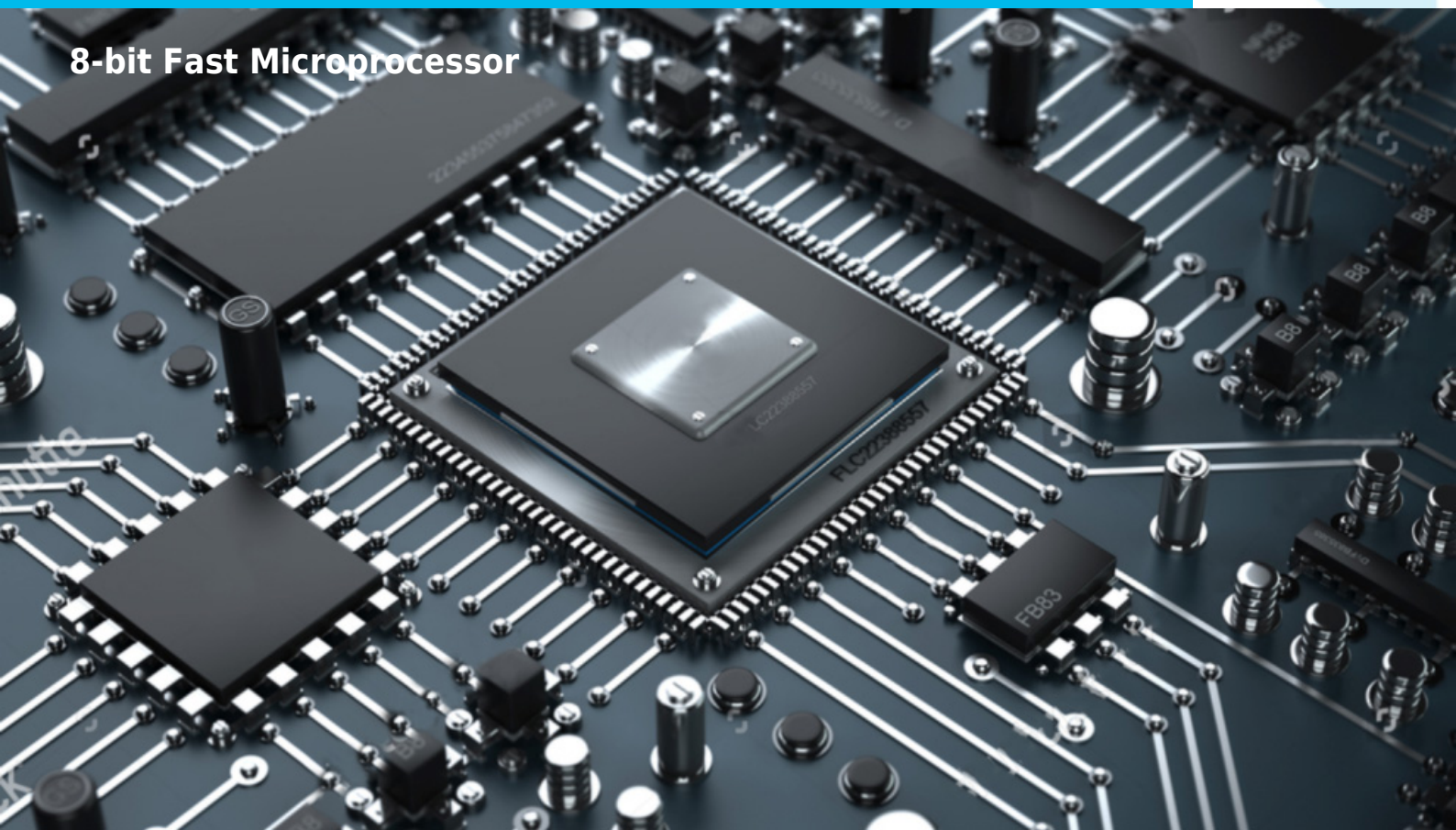
DIGITAL CORE DESIGN

DF6802



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DF6802 is an 8-bit synthesizable MPU IP Core, software-compatible with Motorola MC6802. It has **an enhanced internal architecture** which allows executing the code approximately **4 times faster than the original 6802** running at the same clock frequency. Two software-controlled **power-saving modes** – WAIT and HALT are available to save additional power. These modes make the DF6802 IP Core especially attractive for **automotive and battery-driven applications**. The DF6802 is **fully customizable** – delivered in the exact configuration to meet your requirements. There is no need to pay extra for unused features and wasted silicon. The DF6802 comes with a **fully automated test bench** and a **complete set of tests**, allowing easy package validation at each stage of the SoC design flow. Each DCD's D68XX Core has built-in support for DCD's Hardware Debug System called **DoCD™**. It is a **real-time hardware debugger** that provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides **non-intrusive debugging** of a running application. It can halt, run, step into or skip an instruction, and read/write any contents of the microprocessor.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip, and others.***
- ***TSMC***
- ***UMC***
- ***SK Hynix and others.***

CPU FEATURES

- **Improved, 4 times faster architecture**
- **Software compatible with industry standard MC6802**
- De-multiplexed Address/Data Bus to allow easy memory connection
- Two power saving modes: HALT, WAIT
- Fully synthesizable
- Static synchronous design
- No internal reset generator or gated clock
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

UNITS SUMMARY

Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks. – Performs an opcode decoding instruction and control functions for all other blocks.
DoCD™ – a **real-time hardware debugger** which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal and external program memories, all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off. The separate **DoCD™** clock line, allows debugger to operate in the SLEEP mode (major clock line CLK is stopped).
Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions as well as HALT input pin events.
Interrupt Controller – Responsible for the interrupt manage system, for the processing of the external and internal interrupts and exceptions. It manages auto-vectored interrupt cycles, priority resolving and correct vector numbers creation.
ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index register X and related logic, like arithmetic unit, logic unit, multiplier and divider.
Bus Controller – Program Memory, Data Memory interface controls access into the program and data memories. It contains Program Counter (PC), Stack Pointer (SP) register, and related logic.

PERFORMANCE

To provide you with the most accurate and detailed insights about the ASIC performance, we encourage you to get in touch with us directly.

Please feel free to contact us at **info@dcd.pl**. Our dedicated

team will be more than happy to assist you with any inquiries you may have.

DELIVEVERABLES

- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

CONTACT

Digital Core Design Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/