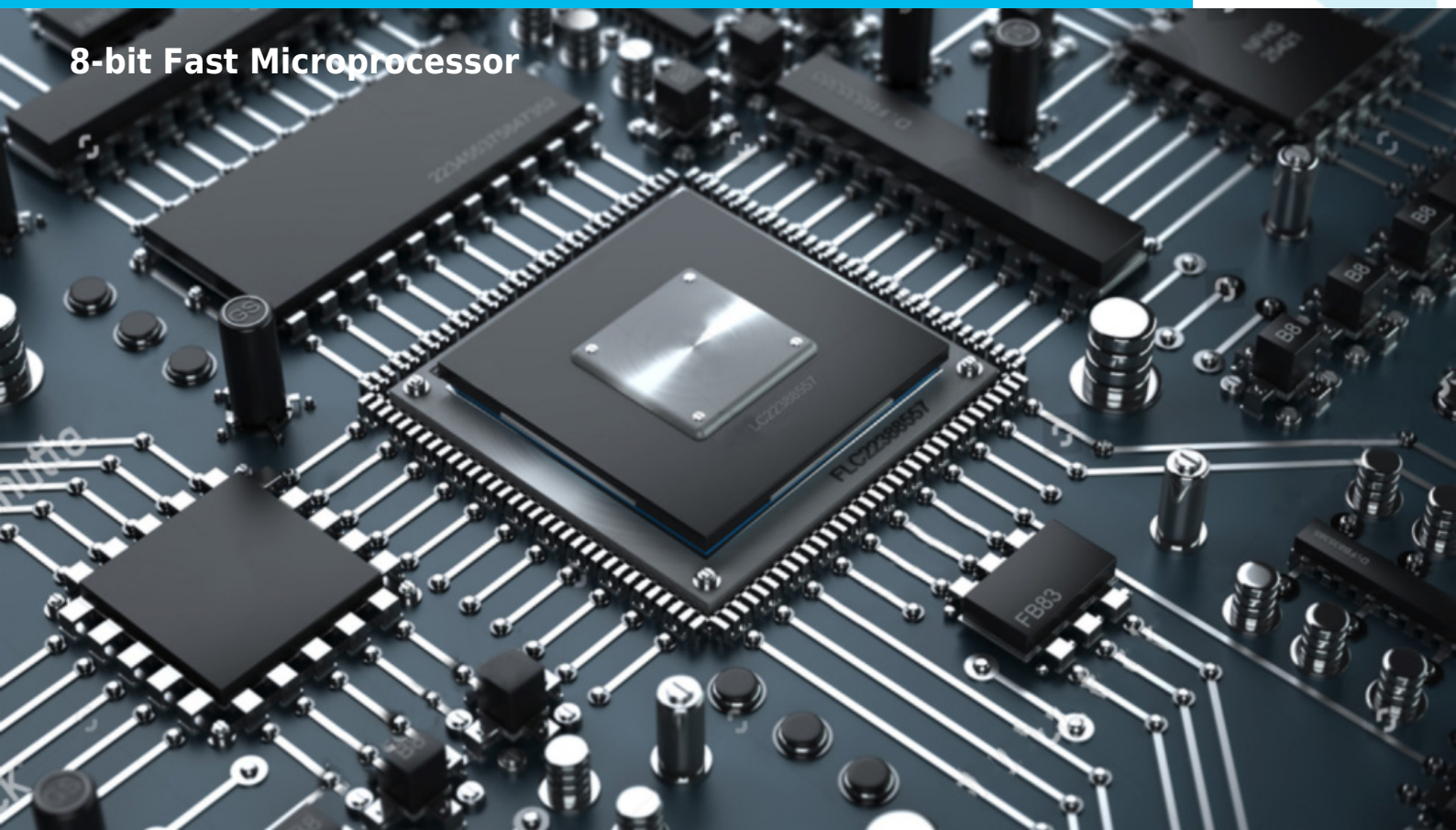
DIGITAL CORE DESIGN

DF6802



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

DF6802 8-bit MPU IP Core – High-Performance, Fully Customizable MC6802 Compatible

The **DF6802** is an 8-bit synthesizable microprocessor IP Core, fully software-compatible with the **Motorola MC6802**. Its enhanced internal architecture allows it to execute code **up to 4× faster** than the original MC6802 at the same clock frequency, making it an ideal choice for **automotive, battery-powered, and industrial SoC applications**.

Designed with energy efficiency in mind, the DF6802 includes **two software-controlled power-saving modes** – **WAIT** and **HALT** – to minimize power consumption, making it perfect for low-power embedded systems.

The DF6802 is **fully customizable**, delivered in an exact configuration to meet your project requirements, avoiding unnecessary silicon and reducing costs. It includes a **fully automated test bench and comprehensive verification suite**, enabling easy package validation at every stage of SoC design.

For advanced debugging, the DF6802 integrates **DCD's DoCD™ Hardware Debug System**, a real-time, non-intrusive debugger capable of halting, running, stepping, and accessing all microprocessor contents, including registers, program memory, and user-defined peripherals.

Key Features & Benefits:

- **MC6802 Compatible:** Run existing software without modification.
- **High Performance:** Executes code up to 4× faster than original MC6802.
- **Low Power:** WAIT and HALT modes for energy-sensitive applications.
- **Customizable:** Include only required features, reducing silicon waste.
- **Automated Validation:** Complete test bench for seamless SoC integration.
- **DoCD™ Debug Support:** Real-time, non-intrusive debugging for faster development.

Applications: Automotive electronics, battery-powered embedded systems, industrial controls, and modern SoC designs requiring MC6802 compatibility with enhanced performance.

D68XX IP Cores Comparison Table

Feature / Core	DF6802	D6802	D6803
Architecture	8-bit synthesizable MPU, enhanced internal architecture	8-bit synthesizable MPU, standard MC6802 architecture	8-bit synthesizable MCU, standard MC6803 architecture with on-chip peripherals
Software Compatibility	Fully compatible with MC6802	Fully compatible with MC6802	Fully compatible with MC6803
Performance	Up to **4× faster** than MC6802 at same clock	Standard performance, same as MC6802	Standard MC6803 performance
Power-Saving Modes	WAIT, HALT	WAIT, HALT	WAIT
Integrated Peripherals	No integrated peripherals (pure MPU)	No integrated peripherals	SCI interface, 16-bit 3-function programmable timer
Customization	Fully customizable to meet project requirements	Fully customizable	Fully customizable
Test Bench & Verification	Fully automated, complete set of tests	Fully automated, complete set of tests	Fully automated, complete set of tests
Hardware Debug Support	DoCD™ real-time, non-intrusive debugger	DoCD™ real-time, non-intrusive debugger	DoCD™ real-time, non-intrusive debugger
Ideal Applications	Automotive, battery-powered embedded systems, industrial SoCs	Automotive, battery-powered embedded systems, industrial SoCs	Automotive, battery-powered embedded systems, industrial SoCs requiring SCI/timers

ALL DCD'S IP CORES ARE TECHNOLOGY AGNOSTIC, ENSURING 100% COMPATIBILITY WITH ALL FPGA AND ASIC VENDORS.

For further details, email info@dcd-semi.com

CPU FEATURES

- **Improved, 4 times faster architecture**
- **Software compatible with industry standard MC6802**
- De-multiplexed Address/Data Bus to allow easy memory

Copyright © 1999 - 2026 DCD - DCD-SEMI Sp. z o.o. All Rights Reserved.
All trademarks mentioned in this document are the property of their respective owners.

connection
- Two power saving modes: HALT, WAIT
- Fully synthesizable
- Static synchronous design
- No internal reset generator or gated clock
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

UNITS SUMMARY

Opcode Decoder – Performs an opcode decoding instruction and control functions for all other blocks. – Performs an opcode decoding instruction and control functions for all other blocks.
DoCD™ – a **real-time hardware debugger** which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, **DoCD™** ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of the microcontroller, including all registers, internal and external program memories, all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off. The separate **DoCD™** clock line, allows debugger to operate in the SLEEP mode (major clock line CLK is stopped).
Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions as well as HALT input pin events.
Interrupt Controller – Responsible for the interrupt manage system, for the processing of the external and internal interrupts and exceptions. It manages auto-vectored interrupt cycles, priority resolving and correct vector numbers creation.
ALU – Arithmetic Logic Unit performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index register X and related logic, like arithmetic unit, logic unit, multiplier and divider.
Bus Controller – Program Memory, Data Memory interface controls access into the program and data memories. It contains Program Counter (PC), Stack Pointer (SP) register, and related logic.

PERFORMANCE

For precise **LATTICE FPGA** performance insights, reach out to us at info@dcd.pl. Our dedicated team is ready to assist you with any inquiries.

DELIVERABLES

- HDL Source Code
- Testbench environment
  - Automatic Simulation macros
  - Tests with reference responses
- Synthesis scripts
- Technical documentation
- 12 months of technical support

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.
– *Single-Site license option* – dedicated to small and middle sized companies which run their business at one place.
– *Remote Access license option* – allows authorized users to access and use the licensed product from a remote location.
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

The IP is delivered in HDL Source code suitable for ASIC and FPGA projects.

CONTACT

DCD-SEMI Sp. z o.o. Headquarters:
Wroclawska 94, 41-902 Bytom, POLAND
E-mail: info@dcd.pl
tel.: +48 32 282 82 66
fax: +48 32 282 74 37
Distributors:
Please check: dcd.pl/contact-us/

Copyright © 1999 - 2026 DCD - DCD-SEMI Sp. z o.o. All Rights Reserved.
All trademarks mentioned in this document are the property of their respective owners.