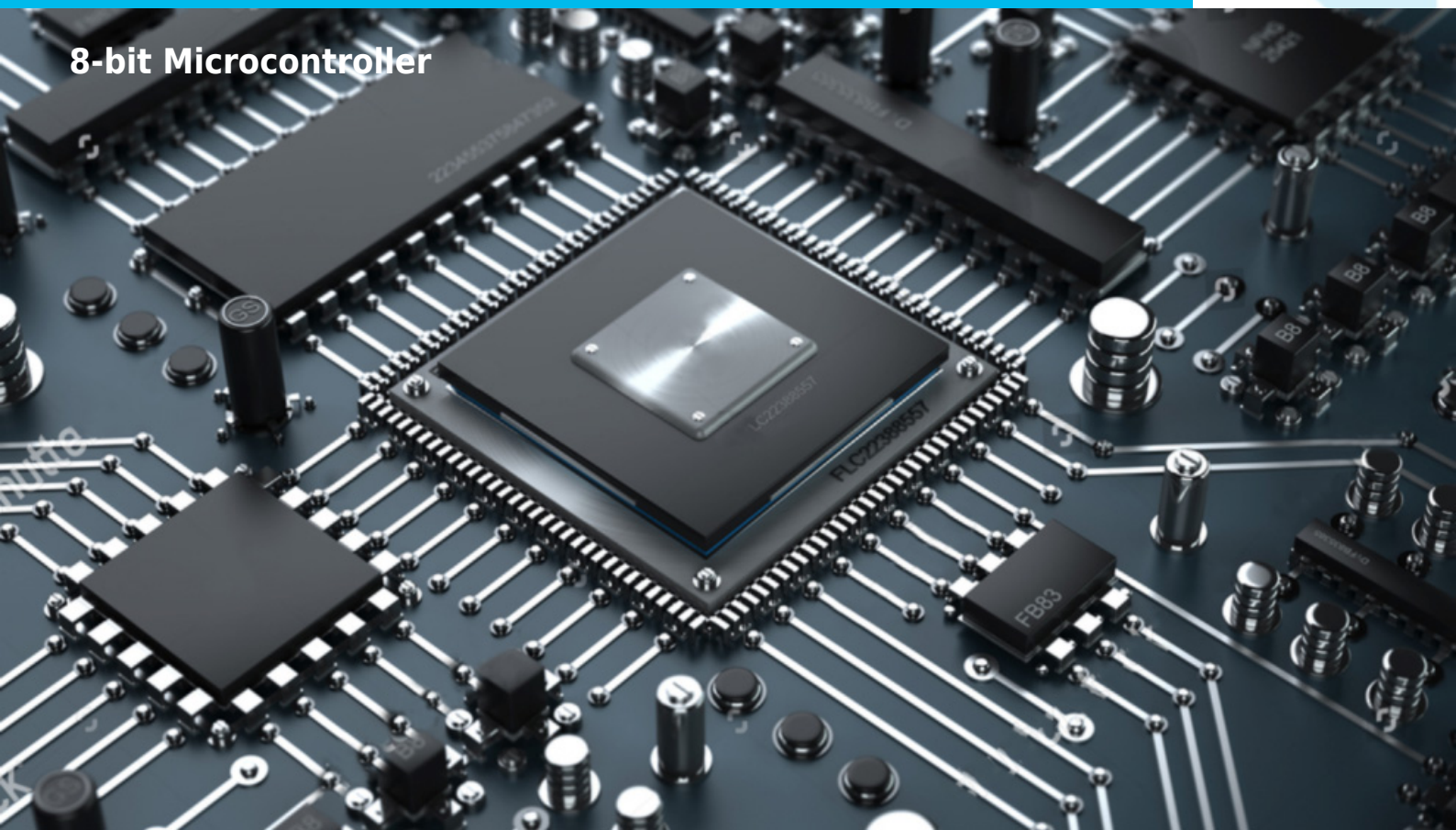
DIGITAL CORE DESIGN

D6803

8-bit Microcontroller



COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The **D6803** is a synthesizable SOFT Microcontroller IP Core, fully compatible with the Motorola MC6803. It can be used as a **direct replacement for MC6803 Microcontrollers.** In the standard configuration, the core has major peripheral functions integrated on-chip. An asynchronous serial communications interface (SCI) is included, as well as the main 16-bit, three-function programmable timer. A software-controlled **power-saving mode** – WAIT is available to save additional power. This mode makes the D6803 IP Core especially attractive for **automotive and battery-driven applications.** DCD's IP Core is **fully customizable** – delivered in the exact configuration to meet your requirements. There is no need to pay extra for unused features and wasted silicon. The IP Core comes with a **fully automated test bench** and a **complete set of tests**, allowing easy package validation at each stage of the SoC design flow. It has built-in support for DCD's Hardware Debug System called **DoCD™** – it is a **real-time hardware debugger** that provides debugging capability of a whole System-on-Chip (SoC). Unlike other on-chip debuggers, the **DoCD™** provides **non-intrusive debugging** of a running application. It can halt, run, step into or skip an instruction, and read/write any contents of the microcontroller, including all registers, and SFRs, including user-defined peripherals and data and program memories.

DESIGN FEATURES:

ALL DCD'S IP CORES ARE TECHNOLOGY INDEPENDENT WHICH MEANS THAT THEY ARE 100% COMPATIBLE WITH ALL FPGA & ASIC VENDORS E.G.

- ***Altera / Intel,***
- ***Xilinx / AMD,***
- ***Lattice,***
- ***Microsemi / Microchip,***
  and others.

- ***TSMC***
- ***UMC***
- ***SK Hynix***
  and others.

CPU FEATURES

- Cycle compatible with original implementation
- Software compatible with 6803 industry standard
- I/O Wrapper making it pin compatiblecore
- Power saving mode: WAIT
- Fully synthesizable
- Static synchronous design
- No internal tri-states
- Scan test ready
- USB, Ethernet, I2C, SPI, UART, CAN, LIN, HDLC, Smart Card interfaces available

DESIGN FEATURES

- One global system clock
- Synchronous reset
- All asynchronous input signals are synchronized before internal use

PERIPHERALS

Peripherals implemented in a standard configuration of the D6803.

- **DoCD™ On-Chip Debugger**
  - Processor execution control
  - Read, write all processor contents
  - Hardware execution breakpoints
- **Three 8-bit and one 5-bit I/O Ports**
- **Extended Interrupt Controller**
- **Main16-bit timer/counter system**
  - 16 bit free running counter
  - Compare/Capture functions
  - Timer clocked by internal source
- **Full-duplex UART – SCI**
  - Standard Non-return to Zero format (NRZ)
  - Integrated baud rate generator
  - Enhanced receiver data sampling technique
  - Overrun and Framing error detection
  - Wake-up block to recognize UART wake-up from IDLE
  - Three SCI related interrupts

OPTIONAL PERIPHERALS

The following optional peripherals can be implemented upon customer's request.

- **ADC Support**
- **Ethernet MAC Controller**
- **CAN, LIN Controllers**
- **I2C bus controller – Master**
- **I2C bus controller – Slave**
- **PWM – Pulse Width Modulation Timer**
- **Fixed-Point arithmetic coprocessor**
- **Floating-Point arithmetic coprocessor IEEE-754 standard single precision**

UNITS SUMMARY

Control Unit – Performs the core synchronization and data flow control. This module manages execution of all instructions.
Opcode Decoder – Performs an instruction opcode decoding and the control functions for all other blocks**.**
ALU – Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index register X and related logic like arithmetic unit, logic unit, multiplier and divider.
Bus Controller – Program Memory, Data Memory interface controls access into the program and data memories. It contains Program Counter (PC), Stack Pointer (SP) register, and related logic.
Interrupt Controller – responsible for the interrupt manage system for the external & internal interrupts and exceptions processing. It manages auto-vectored interrupt cycles, priority resolving and correct vector number creation.
Timer with Compare Capture – The programmable timer is based on free-running 16-bit counter, plus input capture/output compare circuitry. The timer can be used for many purposes, including measuring pulse length of two input signals and generating two output signals. The timer has 16-bit architecture hence each specific functional segment is represented by two 8-bit registers. These registers contain the high and low byte of that functional block. Accessing the low byte of a specific timer function, allows full control of that function, however, an access of the high byte, inhibits that specific timer function until the byte is also accessed. The input-capture channel has its own 16-bit time capture latch (input-capture register) and the output-compare channel has its own 16-bit compare register. Additional control bits permit software to control the edge(s), that trigger each input-capture function and the automatic actions that result from output-compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is mainly a software-oriented system. This structure is easily adaptable to a very wide range of applications, although it is not as efficient, as a dedicated hardware for some specific timing applications.
SCI – a full-duplex UART type asynchronous system, using standard non-return to zero (NRZ) format: 1 start bit and a 1 stop bit. The Core resynchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore, differences in baud rate between the sending device and the SCI are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time and majority logic decides the sense for the bit. The receiver also has the ability to enter a temporary standby mode (called receiver wakeup), to ignore messages intended for a different receiver. Logic automatically wakes the receiver up, in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multi-drop SCI networks. The SCI transmitter can produce queued characters of idle (whole characters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag.
I/O Ports – Three ports are 8-bit general-purpose bidirectional I/O system and one (PORTB) is 5-bit. The PORTA, PORTB, PORTC, PORTD data registers, have their corresponding data direction registers DDRA, DDRB, DDRC, DDRD to control ports data flow. It assures that all D6803's ports have full I/O selectable registers. Writes to any ports pins cause data to be stored in the data registers. If any port pins are configured as output, then data registers are driven out of those pins. Reads from port pins configured as input, causes that input pin is read. If port pins is configured as output, during read data register is read. Writes to any ports pins not configured as outputs, do not cause data to be driven out of those pins, but the data is stored in the output registers. Thus, if the pins later become outputs, the last data written to port, will be driven out the port pins.
DoCD™ Debug Unit – a real-time hardware debugger which provides debugging capability of a whole SoC system. The, **DoCD™** provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller, including all registers, internal, external, program memories, all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed, if any write/read occurs at particular address, with certain data pattern or without pattern. The **DoCD™** system includes three-wire interface and complete set of tools, to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off by the user, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off. The separate CLKDOCD clock line allows the debugger to operate while the CPU is in STOP mode and the major clock line CLK is stopped.

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PERFORMANCE

The following table gives a survey about the Core area and performance in **ASIC** devices (all key features included):

Technology	Optimization	Gates

0.25 typical	area	6 000

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- Source code:
  - VERILOG or VHDL Source Code
  - VERILOG or VHDL test bench environment
    - Active-HDL automatic simulation macros
    - ModelSim automatic simulation macros
    - Tests with reference responses
  - Technical documentation
    - Installation notes
    - HDL core specification
    - Datasheet
  - Synthesis scripts
  - Example application
- Netlist
  - Netlist for selected FPGA family
  - Sample FPGA project
  - Technical documentation
    - HDL core specification
    - Datasheet
- Technical support
  - IP Core implementation
  - 12 months maintenance
    - Delivery of the IP Core and documentation updates
    - Phone & email support
    - Design consulting

LICENSING

Comprehensible and clearly defined licensing methods without royalty-per-chip fees make use of our IP Cores easy and simple.

– Single-Site license option – dedicated to small and middle sized companies which run their business at one place.

– Multi-Site license option – dedicated to corporate customers which operate at several locations. The licensed product can be used at selected company branches.

In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core that you can choose from:
– VHDL or Verilog RTL synthesizable source code (called HDL Source code)
– FPGA EDIF/NGO/NGD/QXP/VQM (called Netlist)

HDL Source code is suitable for ASIC and FPGA projects. The Netlist license is intended for FPGA projects only.

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