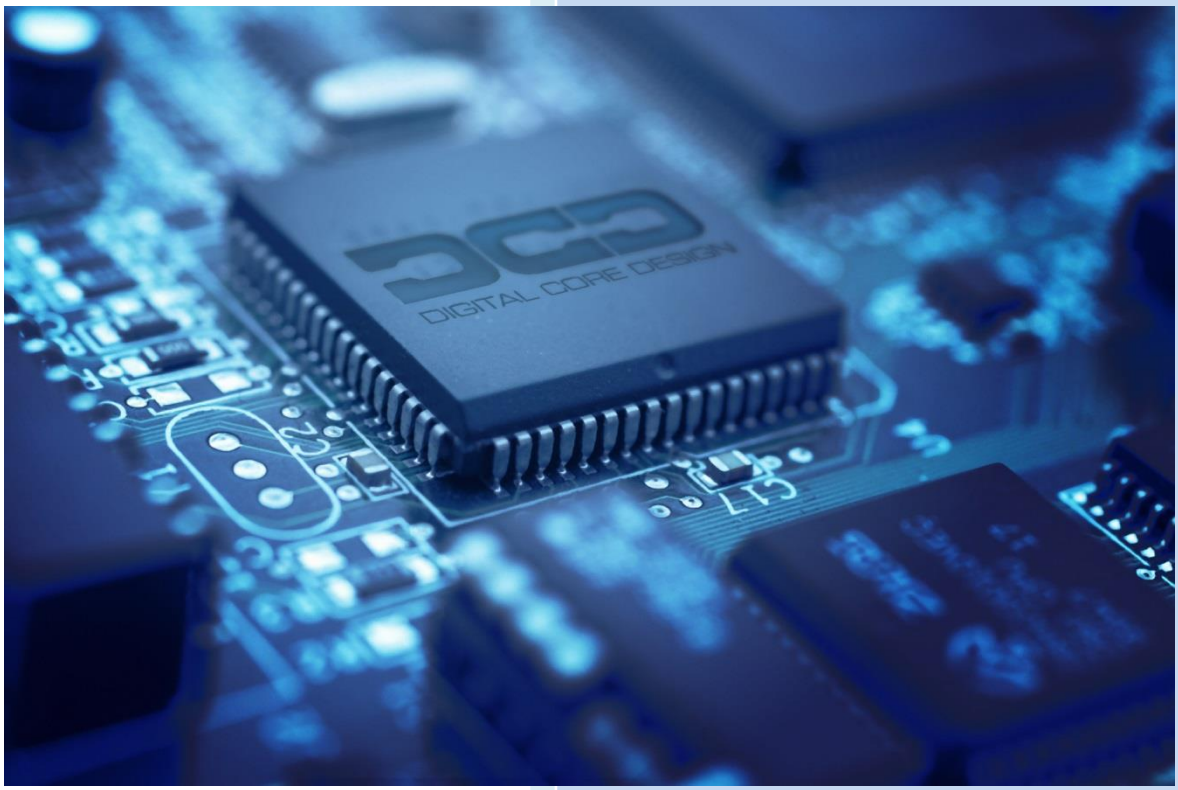
DIGITAL CORE DESIGN

2016

DLCD IP Core



LCD/TFT Display Controller v. 1.10

COMPANY OVERVIEW

Digital Core Design is a leading IP Core provider and a System-on-Chip design house. The company was founded in 1999 and since the very beginning has been focused on IP Core architecture improvements. Our innovative, silicon proven solutions have been employed by over 300 customers and with more than 500 hundred licenses sold to companies like Intel, Siemens, Philips, General Electric, Sony and Toyota. Based on more than 70 different architectures, starting from serial interfaces to advanced microcontrollers and SoCs, we are designing solutions tailored to your needs.

IP CORE OVERVIEW

The DLCD is a display controller, with 24-bit RGB output and synchronization. It may be used for displaying data on LCD or CRT displays. Pixel data has an 8-bit resolution. 24-bit RGB output is generated using external LUT, with defined color palette. The DLCD is controlled by the CPU and uses external memory for data displaying. Display data are accessible for the CPU as an external data memory. The DLCD is a technology independent design that can be implemented in various process technologies.

KEY FEATURES

- Maximum resolution 1024x1024
- 24-bit RGB output, 8-bit pixel with external LUT for color palette
- Configurable screen parameters
- Configurable memory data bus width
- Wait states for memory access
- Pixel clock divider
- Display data copying without CPU access
- Display data accessible for CPU as XDATA memory

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery of the IP Core and documentation updates, minor and major versions changes
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods **without royalty-per-chip fees** make use of our IP Cores easy and simple.

Single-Site license option – dedicated to small and middle sized companies, which run their business in one place.

Multi-Site license option – dedicated to corporate customers, who operate at several locations. The licensed product can be used in selected company branches.

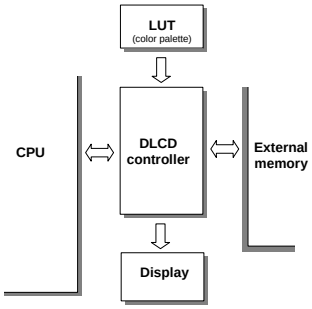
In all cases the number of IP Core instantiations within a project and the number of manufactured chips are unlimited. The license is royalty-per-chip free. There are no restrictions regarding the time of use.

There are two formats of the delivered IP Core:

- VHDL or Verilog RTL synthesizable source code called HDL Source code
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

APPLICATIONS

CPU based applications with LCD/TFT or CRT displays



Typical DLCD and processor connection scheme is shown on the figure above.

UNITS SUMMARY

CPU control – Performs operation of reading and writing internal registers of module.
Sync control – it generates synchronization signals for display and synchronizes data for display.
Memory control – it manages memory access, LUT color palette access, reads pixel data for displaying and controls transactions on external data interface.
Clock divider – it generates divided clock signal for PCLKDIVO output.

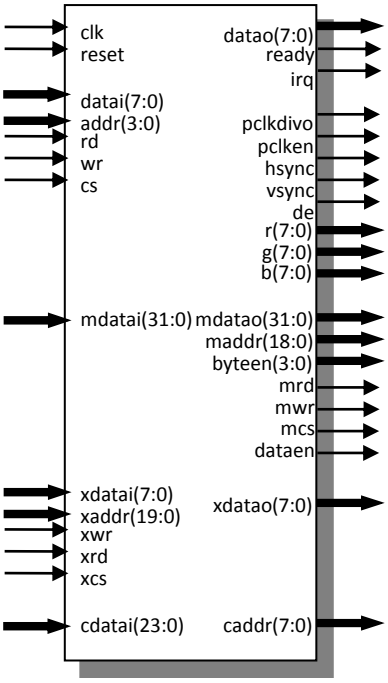
DESIGN FEATURES

The DLCD IP core is, full synchronous with one clock domain, design. All parameters are configurable by CPU. But there is also capability for setting parameters by modification constants in source file. There is no need to wasting silicon resources for unused features and constant settings.

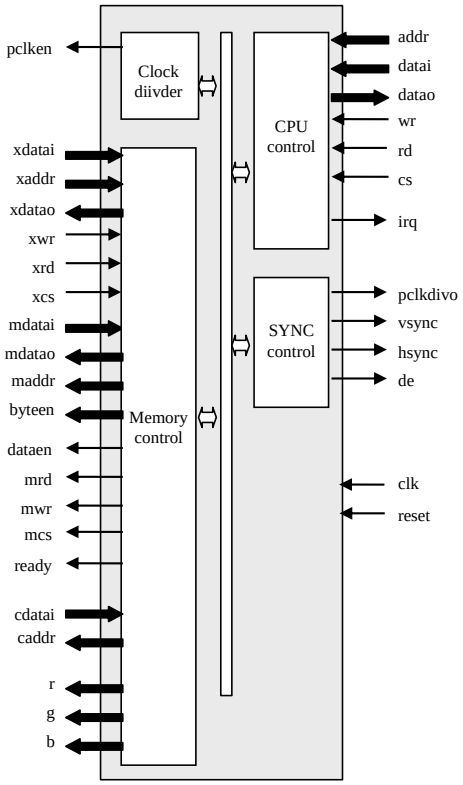
PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Master clock
reset	input	Reset
addr(3:0)	input	CPU interface register address
datai(7:0)	input	CPU interface register data input
rd	input	CPU interface register read control
wr	input	CPU interface register write control
cs	input	CPU interface register chip select
xaddr(19:0)	input	CPU interface XDATA address
xdatai(7:0)	input	CPU interface XDATA data input
xrd	input	CPU interface XDATA read control
xwr	input	CPU interface XDATA write control
xcs	input	CPU interface XDATA chip select
mdatai(31:0)	input	Memory data input bus
cdatai(23:0)	input	Color LUT data input bus
irq	output	Interrupt request output
pclkdivo	output	Divided clock output
pclken	output	Divided Clock enable output
hsync	output	Horizontal synchronization output
vsync	output	Vertical synchronization output
de	output	RGB data valid output
r(7:0)	output	Red color data output bus
g(7:0)	output	Green color data output bus
b(7:0)	output	Blue color data output bus
datao(7:0)	output	CPU interface register data output
maddr(18:0)	output	Memory address
mdatao(31:0)	output	Memory data output bus
byteen(3:0)	output	Byte enable control output
mrd	output	Memory read control output
mwr	output	Memory write control output
dataen	output	Memory data output enable
xdatao(7:0)	output	CPU interface XMEM data output
ready	output	Ready control output
caddr(7:0)	output	Color LUT address

SYMBOL



BLOCK DIAGRAM



PERFORMANCE

The following table gives a survey about the Core area and performance in ALTERA® devices after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	757	148 MHz
CYCLONE 2	-6	751	176 MHz
CYCLONE 3	-6	740	197 MHz
STRATIX	-5	757	156 MHz
STRATIX 2	-3	549	214 MHz
STRATIX 3	-3	548	332 MHz

All features implemented

Core performance in ALTERA® devices

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